

FEATURES

- 8/6/4 Simultaneously Sampled Inputs**
 - True bipolar analog input ranges: $\pm 10\text{ V}$, $\pm 5\text{ V}$**
 - Single 5V Analog Supply, 2.3V to $+5\text{ V}$ V_{DRIVE}**
 - 1M Ω Analog Input Impedance**
 - Analog Input Clamp Protection**
 - 2nd Order Anti-alias Analog Filter**
 - Over-sampling capability with digital filter, e.g. 96dB SNR at 50kSPS**
 - Fast throughput rate: 200 kSPS for all channels**
 - 90dB SNR at 200kSPS**
 - Low power: 80 mW at 200 kSPS, 10 mW per channel**
 - On-chip accurate reference and reference buffer**
 - Flexible Parallel/Serial interface:**
 - SPI[®]-/QSPI[™]-/MICROWIRE[™]-/DSP-compatible**
 - Standby Mode: 6 mW typ**
 - 64-lead LQFP Package**
- ### APPLICATIONS
- Power line monitoring and protection systems**
 - Multiphase Motor Control**
 - Instrumentation and control systems**
 - Multi-axis positioning systems**
 - Data Acquisition Systems**

GENERAL DESCRIPTION

The AD7606¹/AD7606-6/AD7606-4 is a 16-bit, 8/6/4 channel, simultaneous sampling Analog-to-Digital Data Acquisition system (DAS). The parts contains analog input clamp protection, 2nd order anti-alias filter, track and hold amplifier, 16-bit charge redistribution successive approximation ADC, flexible digital filter, 2.5V reference and reference buffer and high speed serial and parallel interfaces.

The AD7606¹/AD7606-6/AD7606-4 operates from a single 5V supply and can accommodate $\pm 10\text{ V}$ and $\pm 5\text{ V}$ true bipolar input signals while sampling at throughput rates up to 200 kSPS for all channels. The input clamp protection circuitry can tolerate voltages up to $\pm 16.5\text{ V}$. The AD7606 has 1 M Ω analog input impedance regardless of sampling frequency. The single supply operation, on chip filtering and high input impedance eliminates the need for driver op-amps and external bipolar supplies. The AD7606¹/AD7606-6/AD7606-4 anti-alias filter has a 3 dB cut off frequency of 22 kHz and provides 40 dB anti-alias rejection when sampling at 200kSPS. The flexible digital filter is pin driven, yields improvements in SNR, and reduces the 3 dB bandwidth.

FUNCTIONAL BLOCK DIAGRAM

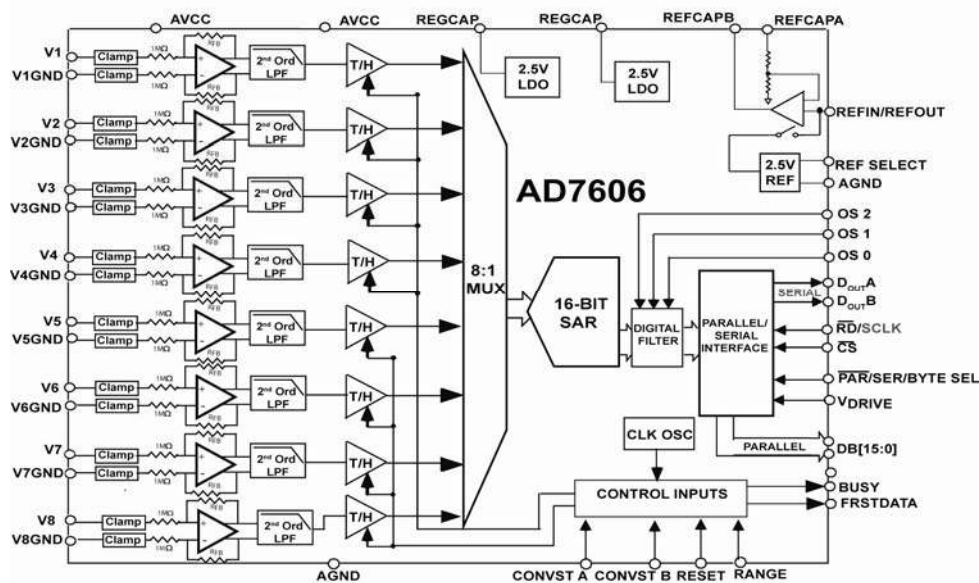


Figure 1.

¹ Patent Pending

Rev. PrL

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REVISION HISTORY

02/10—Revision PrL: Preliminary Version

SPECIFICATIONS

$V_{REF} = 2.5V$ external/internal, $AV_{CC} = 4.75 V$ to $5.25 V$, $V_{DRIVE} = 2.3 V$ to $5.25 V$;
 $f_{SAMPLE} = 200$ kSPS, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.¹

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
	$f_{IN} = 1$ kHz sine wave				
Signal-to-Noise + Distortion (SINAD) ²		88	90		dB
Signal-to-Noise Ratio (SNR) ²		88	90		dB
OS rate x 8 (25 ksp/s) (see Digital filter Section)		95	96		dB
Total Harmonic Distortion (THD) ²			-105	-95	dB
Peak Harmonic or Spurious Noise (SFDR) ²			-100		dB
Intermodulation Distortion (IMD) ²	$f_a = 1$ kHz, $f_b = 1.1$ kHz				
Second-Order Terms			-112		dB
Third-Order Terms			-107		dB
Channel-to-Channel Isolation ²	f_{IN} on unselected channels up to TBD kHz		-100		dB
ANALOG INPUT FILTER					
Full Power Bandwidth	@ -3 dB $\pm 10V$ range		22		kHz
	@ -3 dB $\pm 5V$ range		14		kHz
	@ -0.1 dB $\pm 10V$ range		12		kHz
	@ -0.1 dB $\pm 5V$ range		5		kHz
$t_{GROUP DELAY}$			16		us typ
$t_{GROUP DELAY}$ matching across all channels			TBD		ns typ
DC ACCURACY					
Resolution	No Missing Codes	16			Bits
Differential Nonlinearity ²			± 0.5	± 0.95	LSB
Integral Nonlinearity ²			± 0.5	± 2	LSB
Positive Full-Scale Error ²	External reference		± 1	± 40	LSB
	Internal reference		$\pm TBD$		LSB
Positive Full-Scale Error Drift ²	External reference		5		ppm/ $^{\circ}C$
	Internal reference		± 15		ppm/ $^{\circ}C$
Positive Full-Scale Error Matching ²	Internal/External reference		1	20	LSB
Bipolar Zero-Scale Error ²	Internal/External reference (for full AD7606 signal Chain)		± 1	± 10	LSB
Bipolar Zero-Scale Error drift ²	Internal/External reference		TBD		$\mu V/^{\circ}C$
Bipolar Zero-Scale Error Matching ²	Internal/External reference		1	5	LSB
Negative Full-Scale Error ²	External reference		± 1	± 40	LSB
	Internal reference		$\pm TBD$		LSB
Negative Full-Scale Error Drift ²	External reference		5		ppm/ $^{\circ}C$
	Internal reference		± 15		ppm/ $^{\circ}C$
Negative Full-Scale Error Matching ²	Internal/External reference		1	20	LSB
ANALOG INPUT					
Input Voltage Ranges	RANGE = 1			± 10	V
	RANGE = 0			± 5	V
DC Leakage Current	Analog input $\pm 16.5V$			± 1	μA
Input Capacitance ³			5		pF
Input Impedance	See Analog input section		1		M Ω
REFERENCE INPUT/OUTPUT					
Reference Input Voltage Range	See ADC Transfer Function	TBD	2.5	TBD	V
DC Leakage Current				± 1	μA
Input Capacitance ³	REF SELECT= 1		9.5		pF
Reference Output Voltage	REFIN/REFOUT	TBD	2.5	TBD	V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Reference Temperature Coefficient			±10		ppm/°C
LOGIC INPUTS					
Input High Voltage (V_{INH})	Typically 10 nA, $V_{IN} = 0\text{ V}$ or V_{DRIVE}	$0.7 \times V_{DRIVE}$			V
Input Low Voltage (V_{INL})				$0.3 \times V_{DRIVE}$	V
Input Current (I_{IN})				±1	µA
Input Capacitance (C_{IN}) ³				5	pF
LOGIC OUTPUTS					
Output High Voltage (V_{OH})	$I_{SOURCE} = 200\ \mu\text{A}$	$V_{DRIVE} - 0.2$			V
Output Low Voltage (V_{OL})	$I_{SINK} = 200\ \mu\text{A}$			0.2	V
Floating-State Leakage Current				±10	µA
Floating-State Output Capacitance ³				10	pF
Output Coding	2's Complement				
CONVERSION RATE					
Conversion Time	All 8 channels included			4	µs
Track-and-Hold Acquisition Time ^{2,3}				1	µs
Throughput Rate	Per channel, all 8 channels included			200	kSPS
POWER REQUIREMENTS					
A_{VCC}		4.75		5.25	V
V_{DRIVE}		2.3		5.25	V
I_{TOTAL}	Digital I/Ps = 0 V or V_{DRIVE}				
Normal Mode (Static)	AD7606		15	19	mA
	AD7606-6		TBD	TBD	mA
	AD7606-4		TBD	TBD	mA
Normal Mode (Operational)	$f_{SAMPLE} = 200\text{ kSPS}$, AD7606		16	21	mA
	$f_{SAMPLE} = 200\text{ kSPS}$, AD7606-6		TBD	TBD	mA
	$f_{SAMPLE} = 200\text{ kSPS}$, AD7606-4		TBD	TBD	mA
Standby Mode			1.2	1.4	mA
Shutdown Mode			1	5	µA
Power Dissipation					
Normal Mode (Static)			75	100	mW
Normal Mode (Operational)	$f_{SAMPLE} = 200\text{ kSPS}$ AD7606		80	110	mW
	AD7606-6			TBD	mW
	AD7606-4			TBD	mW
Standby Mode			6	7.35	mW
Shutdown Mode			TBD	TBD	µW

¹ Temperature range for B version is -40°C to +85°C.

² See the Terminology section.

³ Sample tested during initial release to ensure compliance.

TIMING SPECIFICATIONS

$V_{CC} = 4.75\text{ V to }5.25\text{ V}$, $V_{DRIVE} = 2.3\text{ V to }5.25\text{ V}$, $V_{REF} = 2.5\text{ V}$ external reference/ internal reference,
 $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.¹

Table 2.

Parameter	Limit at T_{MIN} , T_{MAX}		Unit	Description
PARALLEL/ SERIAL MODE				
Parameter	min	max	Unit	Description
t_{CYCLE}		5	μs	$1/f_{CONVST}$ CONVST cycle time (throughput time) SERIAL MODE – applies for reading during a conversion only
t_{CONV}		TBD		SERIAL MODE – reading after a conversion
		4	μs	Conversion time, internal clock. Oversampling Off. AD7606
		3	μs	AD7606-6
		2	μs	AD7606-4
	TBD	TBD	μs	Over sampling by 2
	TBD	TBD	μs	Over sampling by 4
	TBD	TBD	μs	Over sampling by 8
$t_{WAKE-UP STANDBY}$	TBD	TBD	μs	Over sampling by 16
	TBD	TBD	μs	Over sampling by 32
	TBD	TBD	μs	Over sampling by 64
		100	μs	\overline{STBY} rising edge to CONVST rising edge. Power up time from standby mode.
		11	ms	\overline{STBY} rising edge to CONVST rising edge. Power up time from shutdown mode. Internal Reference
		11	ms	\overline{STBY} rising edge to CONVST rising edge. Power up time from shutdown mode. External Reference
t_{RESET}	100		ns	RESET high pulse width.
t_1		60	ns	CONVST high to BUSY high
t_2	25		ns	Minimum CONVST low pulse
t_3	25		ns	Minimum CONVST high pulse
t_4	0		ns	BUSY falling edge to CS falling edge set-up time
t_5		TBD	ns	Maximum delay allowed between CONVSTA/B rising edges
t_6		TBD	ns	Maximum time between last \overline{CS} rising edge and BUSY falling edge.
t_7	TBD		ns	Minimum delay between RESET low to CONVST high
t_8	10		ns	BUSY to OS x pin setup time
t_9	10		ns	BUSY to OS x pin hold time
PARALLEL READ OPERATION				
t_8	0		ns	\overline{CS} to \overline{RD} setup time
t_9	0		ns	\overline{CS} to \overline{RD} hold time
t_{10}	20		ns	\overline{RD} low pulse width
t_{11}				Data access time after \overline{RD} falling edge
		20	ns	$V_{DRIVE} = 5.25\text{ V}$
		TBD	ns	$V_{DRIVE} = 4.75\text{ V}$
		TBD	ns	$V_{DRIVE} = 3.6\text{ V}$
		TBD	ns	$V_{DRIVE} = 2.7\text{ V}$
	TBD	ns	$V_{DRIVE} = 2.3\text{ V}$	
t_{12}	7		ns	Data hold time after \overline{RD} rising edge
t_{13}	10		ns	\overline{RD} high pulse width
t_{14}	12		ns	\overline{CS} high pulse width (Figure 5) \overline{CS} and \overline{RD} linked
t_{15}		12	ns	Delay from \overline{CS} rising edge to DB[15:0] three-state enabled

t ₁₆	TBD		ns	\overline{CS} to DB[15:0] hold time
t ₁₇		9.5	ns	Delay from \overline{CS} until DB[15:0] three-state disabled
t ₁₈		10	ns	\overline{RD} falling edge to FRSTDATA high
t ₁₉		10	ns	\overline{RD} falling edge to FRSTDATA low
SERIAL READ OPERATION				
f _{SCLK}		40	MHz max	Frequency of serial read clock
t ₂₀		9.5	ns	Delay from \overline{CS} until D _{OUTA} / D _{OUTB} three-state disabled
t ₂₁ ²		9.5	ns	Delay from \overline{CS} until MSB valid
				Data access time after SCLK rising edge
		20	ns	V _{DRIVE} = 5.25V
		TBD	ns	V _{DRIVE} = 4.75V
		TBD	ns	V _{DRIVE} = 3.6 V
		TBD	ns	V _{DRIVE} = 2.7 V
		TBD	ns	V _{DRIVE} = 2.3 V
t ₂₂	10		ns	SCLK low pulse width
t ₂₃	10		ns	SCLK high pulse width
t ₂₄	7		ns	SCLK falling edge to D _{OUTA} / D _{OUTB} valid hold time
t ₂₅		12	ns	\overline{CS} rising edge to D _{OUTA} / D _{OUTB} three-state enabled
t ₂₆		10	ns	16 th SCLK falling edge to FRSTDATA low
t ₂₈	0		ns	Delay from \overline{CS} rising edge until FRST three-state enable
t ₂₉	15		ns	Delay from \overline{CS} falling edge until FRST three-state disabled
t ₃₀	10		ns	Delay from \overline{CS} falling edge until FRST high SERIAL MODE
PARALLEL BYTE MODE				
t ₃₁	0		ns	HBEN to \overline{RD} setup time
t ₃₂	0		ns	HBEN to \overline{RD} hold time

¹ Sample tested during initial release to ensure compliance. All input signals are specified with t_r = t_f = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.

² A buffer is used on the data output pins for this measurement.

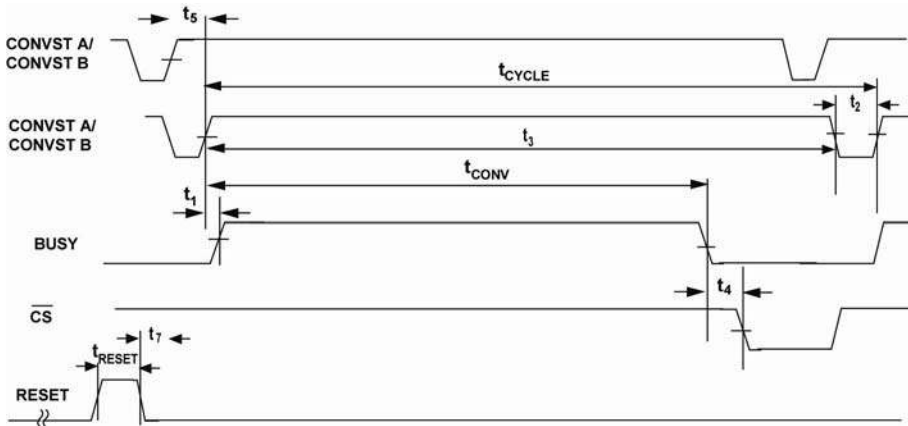


Figure 2. CONVST timing – Reading after a conversion

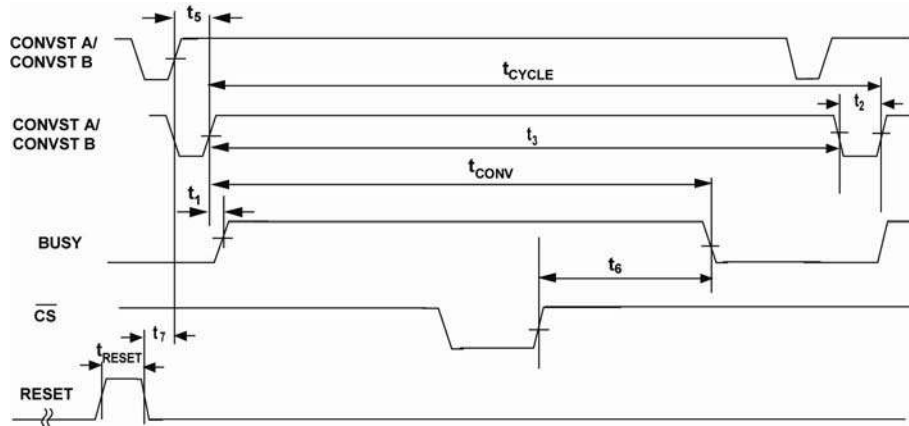


Figure 3. CONVST timing – reading during a conversion

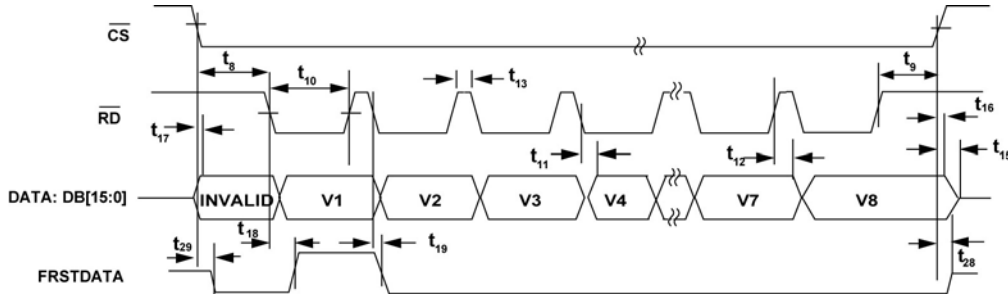


Figure 4 Parallel Mode Separate $\overline{\text{CS}}$ and $\overline{\text{RD}}$ pulses

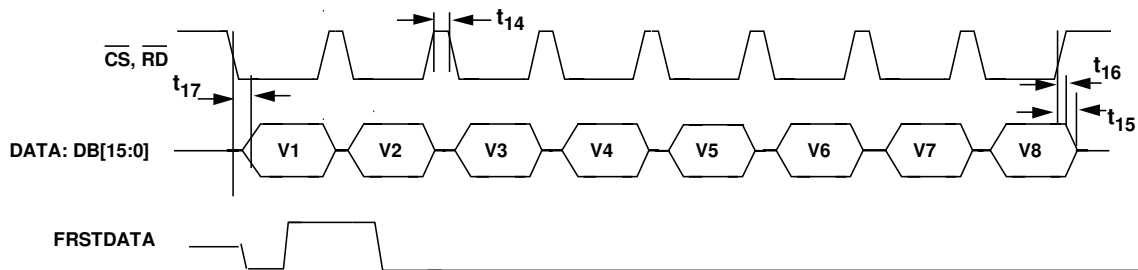


Figure 5. $\overline{\text{CS}}$ and $\overline{\text{RD}}$ linked Parallel Mode

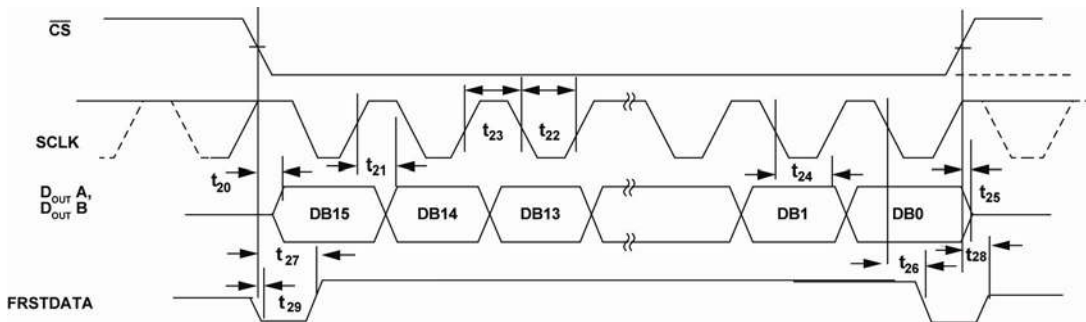


Figure 6. Serial Read Operation (Channel 1)

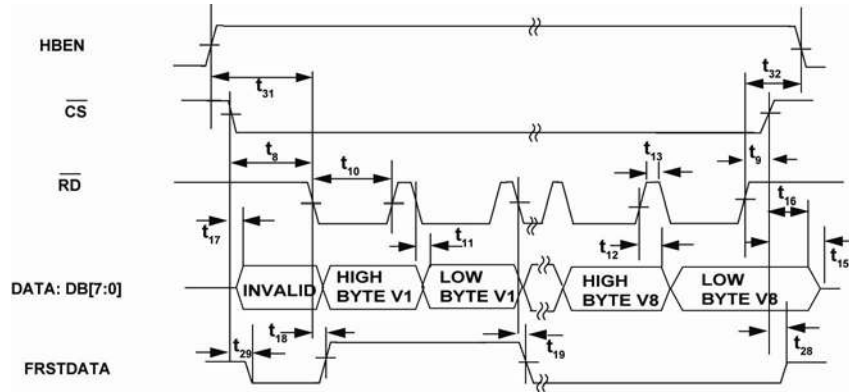


Figure 7. BYTE mode read operation

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted

Table 3.

Parameter	Rating
AV _{CC} to AGND, DGND	−0.3 V to +7 V
AGND to DGND	−0.3 V to +0.3 V
V _{DRIVE} to DGND	−0.3 V to +AV _{CC} + 0.3 V
Analog Input Voltage to AGND ¹	±16.5V
Digital Input Voltage to DGND	−0.3 V to V _{DRIVE} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V _{DRIVE} + 0.3 V
REFIN to AGND	−0.3 V to AV _{CC} + 0.3 V
Input Current to Any Pin Except Supplies ¹	±10 mA
Operating Temperature Range B Version	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Pb/SN Temperature, Soldering Reflow (10 sec to 30 sec)	240(+0)°C
Pb-Free Temperature, Soldering Reflow	260(+0)°C
ESD (all pins except Analog Inputs)	2 kV
ESD (analog Input pins only)	7 kV

¹ Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. These specifications apply to a four-layer board.

Table 4. Thermal Resistance

Package Type	θ _{JA}	θ _{JC}	Unit
64 LQFP	45	11	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

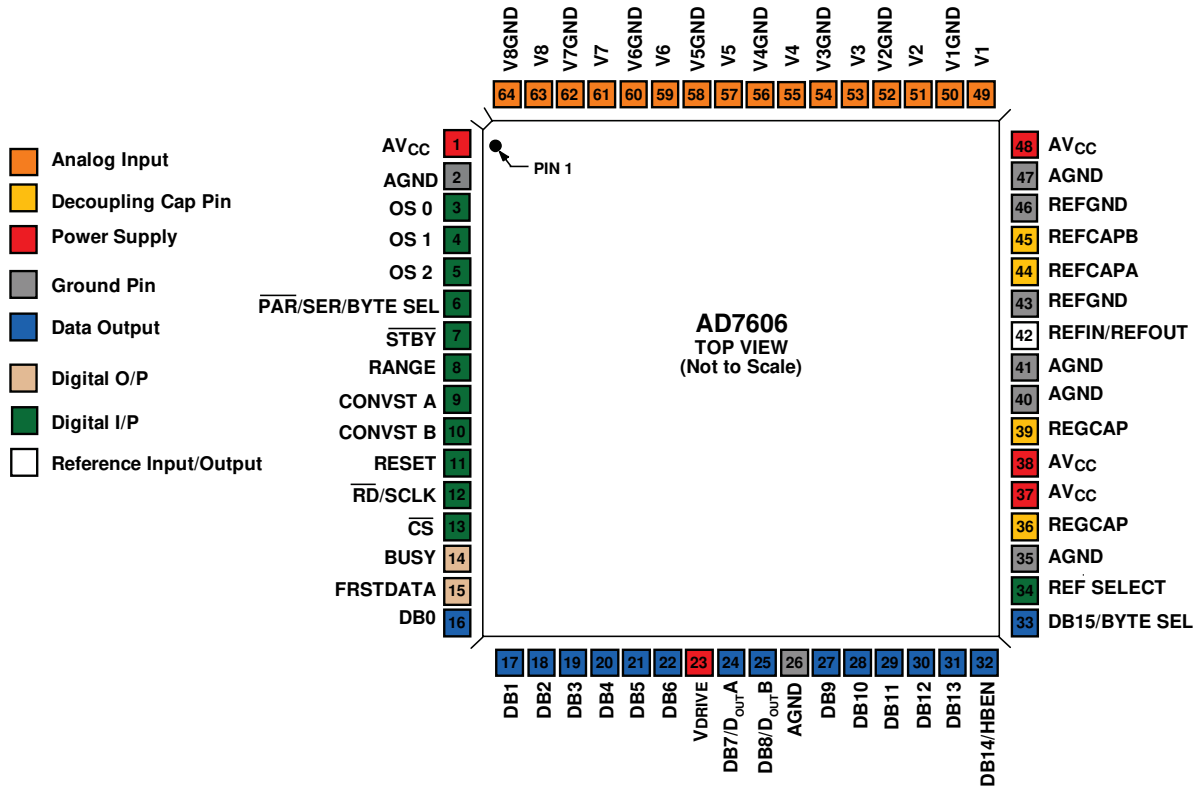


Figure 8. AD7606 Pin Configuration

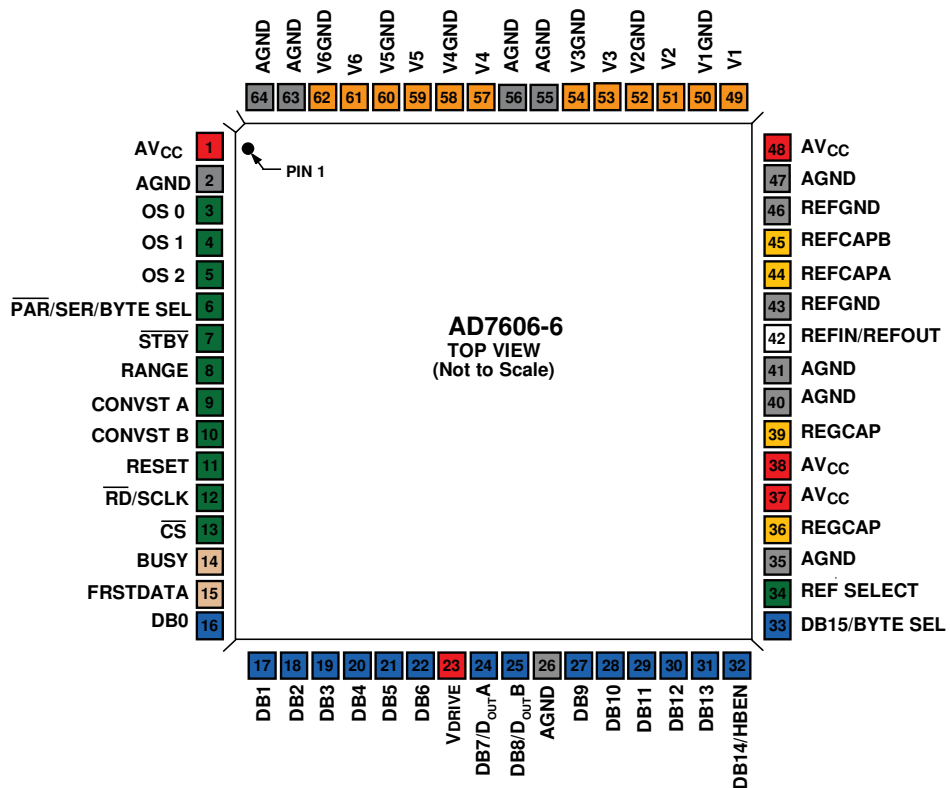


Figure 9. AD7606-6 Pin Configuration

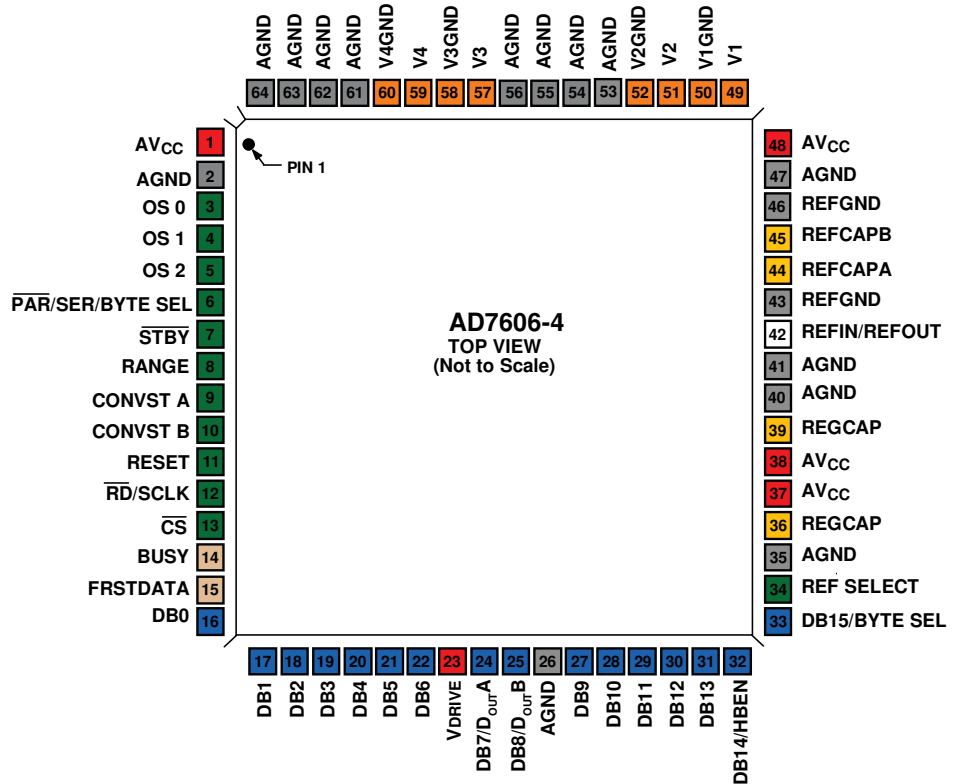


Figure 10. AD7606-4 Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Type ¹	Mnemonic			Description
		AD7606	AD7606-6	AD7606-4	
1, 37, 38, 48	P	AV _{CC}	AV _{CC}	AV _{CC}	Analog Supply Voltage 4.75V to 5.25V. This supply voltage is applied to the internal front end amplifiers and to the ADC core. These supply pins should be decoupled to AGND.
2, 26, 35, 40, 41, 47	P	AGND	AGND	AGND	Analog ground. This pin is the ground reference point for all analog circuitry on the AD7606. All analog input signals and external reference signals should be referred to these pins. All six of these AGND pins should connect to the AGND plane of a system.
23	P	V _{DRIVE}	V _{DRIVE}	V _{DRIVE}	Logic Power Supply Input. The voltage (2.3V to 5V) supplied at this pin determines the operating voltage of the interface. This pin is nominally at the same supply as the supply of the host interface (i.e. DSP, FPGA).
36, 39	P	REGCAP	REGCAP	REGCAP	Decoupling capacitor pins for voltage output from internal regulator. These output pins should be decoupled separately to AGND using a 1µF capacitor. The voltage on these output pins is in the range of 2.5V to 2.7V.
49	A.I.	V1	V1	V1	Analog Inputs. These pins are single-ended analog inputs. The analog input range of these channels is determined by the RANGE pin
51	A.I.	V2	V2	V2	Analog Inputs. These pins are single-ended analog inputs. The analog input range of these channels is determined by the RANGE pin
53	A.I./GND	V3	V3	AGND	Analog input 3. For the AD7606-4 this is an AGND pin.
55	A.I./GND	V4	AGND	AGND	Analog input 3. For the AD7606-4 and the AD7606-6 this is an AGND pin.

¹Refers to classification of pin type; P denotes power, A.I. denotes analog input, REF denotes reference, D.I. denotes digital input, D.O. denotes digital output.

Pin No.	Type ¹	Mnemonic			Description
		AD7606	AD7606-6	AD7606-4	
57	A.I.	V5	V4	V3	Analog Inputs. These pins are single-ended analog inputs. The analog input range of these channels is determined by the RANGE pin
59	A.I.	V6	V5	V4	Analog Inputs. These pins are single-ended analog inputs.
61	A.I./GND	V7	V6	AGND	Analog Input pins. For the AD7606-4 this is an AGND pin.
63	A.I./GND	V8	AGND	AGND	Analog Input pin. For the AD7606-4 and AD7606-6 this is an AGND pin.
50, 52,,	A.I. GND	V1GND & V2GND	V1GND & V2GND	V1GND & V2GND	Analog input ground pins corresponding to the analog input pins V1 and V2. All Analog input AGND pins should connect to the AGND plane of a system.
54	A.I. GND/ GND	V3GND	V3GND	AGND	Analog Input ground pin. For the AD7606-4 this is an AGND pin.
56	A.I. GND/ GND	V4GND	AGND	AGND	Analog Input ground pin. For the AD7606-4 and AD7606-6 this is an AGND pin.
58	A.I. GND/ GND	V5GND	V4GND	V3GND	Analog input ground pins. All Analog input AGND pins should connect to the AGND plane of a system.
60	A.I. GND/ GND	V6GND	V5GND	V4GND	Analog input ground. All Analog input AGND pins should connect to the AGND plane of a system.
62	A.I. GND/ GND	V7GND	V6GND	AGND	Analog Input ground pin. For the AD7606-4 this is an AGND pin.
64.	A.I. GND/ GND	V8GND	AGND	AGND	Analog Input ground pin. For the AD7606-4 and AD7606-6 this is an AGND pin.
42	REF	REFIN/ REFOUT	REFIN/ REFOUT	REFIN/ REFOUT	Reference Input/ Reference Output. The gained up on-chip reference of 2.5V is available on this pin for external use if the REF SELECT pin is set to a logic high. Alternatively, the internal reference can be disabled by setting the REF SELECT pin to a logic low and an external reference of 2.5V can be applied to this input. See the Internal/external Reference section. Decoupling is required on this pin for both the internal or external reference options. A 10 uF capacitor should be applied from this pin to ground close to the REFGND pins.
34	D.I.	REF SELECT	REF SELECT	REF SELECT	Internal/ External reference selection input. Logic input. If this pin is set to logic high then the internal reference is selected and is enabled, if this pin is set to logic low then the internal reference is disabled and an external reference voltage must be applied to the REFIN/REFOUT pin.
44, 45	REF	REFCAPA, REFCAPB	REFCAPA, REFCAPB	REFCAPA, REFCAPB	Reference buffer output force/sense pins. These pins must be connected together and decoupled to AGND using a low ESR 10µF ceramic capacitor.
43, 46	REF	REFGND	REFGND	REFGND	Reference ground pins. These pins should be connected to AGND.
8	D.I.	RANGE	RANGE	RANGE	Analog Input Range Selection. Logic input. The polarity on this pin determines the input range of the analog input channels. If this pin is tied to a logic high, the analog input range is ±10V for all channels. If this pin is tied to a logic low, the analog input range is ±5V for all channels. A logic change on this pin will have an immediate effect on the analog input range. Changing this pin during a conversion is not recommended. See Analog Input section for more details.
6	D.I.	PAR /SER/BYTE SEL	PAR /SER/BYTE SEL	PAR /SER/BYTE SEL	Parallel/serial/byte interface selection input. Logic input. If this pin is tied to a logic low, the parallel interface is selected. If this pin is tied to a logic high, the serial interface is selected. Byte interface mode is selected when this pin is a logic high and when DB 15/BYTE SEL is logic high. Table 8 SERIAL MODE: RD/SCLK pin functions as the Serial Clock input. DB7/D _{OUT} A pin functions as a Serial Data Output.. DB8/D _{OUT} B pin functions as a Serial Data Output.. When the serial interface is selected pins DB[15:9] and DB[6:0] should be tied to GND. BYTE MODE:

Pin No.	Type ¹	Mnemonic			Description
					DB15 in conjunction with $\overline{\text{PAR/SER/BYTE SEL}}$ is used to selected the parallel byte mode of operation. (See Table 8) DB14 is used as HBEN pin. DB[7:0] will transfer the 16 bit conversion result in $2 \overline{\text{RD}}$ operations. DB0 will be the LSB of the data transfers.
9, 10	D.I.	CONVST A CONVST B	CONVST A CONVST B	CONVST A CONVST B	Conversion Start Input A, Conversion Start Input B. Logic inputs. These logic inputs are used to initiate conversions on the analog input channels. For simultaneous sampling of all input channels CONVST A and CONVST B can be shorted together and a single convert start signal applied. Alternatively, CONVST A can be used to initiate simultaneous sampling for (V1, V2, V3 and V4) for AD7606, (V1, V2, V3) for AD7606-6 and (V1 and V2) for the AD7606-4 and CONVST B can be used to initiate simultaneous sampling on the other analog inputs; (V5, V6, V7 and V8) for the AD7606, (V4, V5, V6) for the AD7606-6 and (V3 and v4) for the AD7606-4. This is only possible when oversampling is not switched on. When the CONVST A or CONVST B pins transitions from low to high, the front end track and hold circuitry for their respective analog inputs is set to hold. This function allows a phase delay to be created inherently between the sets of analog inputs.
13	D.I.	$\overline{\text{CS}}$	$\overline{\text{CS}}$	$\overline{\text{CS}}$	Chip Select. This active low logic input frames the data transfer. When both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are logic low in parallel mode, the output bus DB[15:0] is enabled and the conversion result is output on the parallel data bus lines. In serial mode, the $\overline{\text{CS}}$ is used to frame the serial read transfer and clock out the MSB of the serial output data.
12	D.I.	$\overline{\text{RD/SCLK}}$	$\overline{\text{RD/SCLK}}$	$\overline{\text{RD/SCLK}}$	Parallel Data Read control input when parallel interface selected. Serial clock input when the serial interface is selected. When both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are logic low in parallel mode, the output bus is enabled. In serial mode this pin acts as the serial clock input for data transfers. The $\overline{\text{CS}}$ falling edge takes the data output lines DOUTA and DOUTB out of tri-state and clocks out the MSB of the conversion result. The rising edge of SCLK clocks all subsequent data bits onto the serial data outputs DOUTA and DOUTB. For further information see Conversion Control.
14	D.O.	BUSY	BUSY	BUSY	Busy Output. This pin transitions to a logic high after both CONVST A and CONVST B rising edges and indicates that the conversion process has started. The BUSY output remains high until the conversion process for all channels is complete. The falling edge of BUSY signals that the conversion data is being latched into the output data registers and will be available to be read after a time t_4 . Any data read while BUSY is high should be complete before the falling edge of BUSY occurs (subject to t_{QUIET} unread data will be lost. Rising edges on CONVST A or CONVST B will have no effect whilst the BUSY signal is high.
11	D.I.	RESET	RESET	RESET	RESET input. When set to logic high, the rising edge of RESET resets the AD7606/AD7606-6/AD7606-4. The part should receive a RESET pulse after power-up. The RESET high pulse should be typically 100 ns wide. If a RESET pulse is applied during a conversion then the conversion is aborted. If a RESET pulse is applied during a read then the contents of the output registers will reset to all zeros.
15	D.O.	FRSTDATA	FRSTDATA	FRSTDATA	Digital output. The FRSTDATA output signal indicates when the first channel, V1, is being read back on either the parallel, byte or serial interface. When the $\overline{\text{CS}}$ input is high the FRSTDATA output pin is in three-state. The falling edge of $\overline{\text{CS}}$ takes FRSTDATA out of three-state. In parallel mode the falling edge of $\overline{\text{RD}}$ corresponding to the result of V1 will then set the FRSTDATA pin high indicating that the result from V1 is available on the output data bus. The FRSTDATA output returns to a logic low following the next falling edge of $\overline{\text{RD}}$. In serial mode FRSTDATA will go high on the falling edge of $\overline{\text{CS}}$ as this clocks out the MSB of V1 on DOUTA. It returns low on the sixteenth SCLK falling edge after the $\overline{\text{CS}}$ falling edge. See Conversion Control for more details.

Pin No.	Type ¹	Mnemonic			Description
		AD7606	AD7606-6	AD7606-4	
7	D.I.	STBY	STBY	STBY	Standby Mode Input. This pin is used to place the AD7606 into one of two power-down modes, Standby mode or Shutdown mode. The power-down mode entered depends on the state of the RANGE pin as shown in Table 7. When in Standby mode all circuitry except the on-chip reference, regulators and regulator buffers is powered down. When in Shutdown mode all circuitry is powered down.
3,4,5	D.I.	OS [2: 0]	OS [2: 0]	OS [2: 0]	Over-sampling mode pins. Logic inputs. These inputs are used to select the over-sampling ratio. OS 2 is the MSB control bit while OS 0 is the LSB control bit. See the Digital filter section for further details on the over-sampling mode of operation and Table 9 for over-sampling bit decoding.
33	D.O./D.I.	DB15/ BYTE SEL	DB15/ BYTE SEL	DB15/ BYTE SEL	Parallel output data bits, Data Bit15/Parallel Byte Mode select. When $\overline{\text{PAR/SER SEL}} = 0$, this pins act as three-state parallel digital output pin. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low, this pin is used to output DB15 of the conversion result. When $\overline{\text{PAR/SER SEL}} = 1$, BYTE SEL pin is used to select between the Serial Interface mode or Parallel Byte Mode. See Table 8. When $\overline{\text{PAR/SER SEL}} = 1$ and DB15/BYTE SEL = 0 the AD7606 will operate in Serial interface mode. When $\overline{\text{PAR/SER SEL}} = 1$ and DB15/BYTE SEL = 1 the AD7606 will operate in parallel byte interface mode.
32	D.O./D.I.	DB14/HBE N	DB14/HBEN	DB14/HBEN	Parallel output data bits, Data Bit14/High Byte Enable. When $\overline{\text{PAR/SER SEL}} = 0$, this pins act as three-state parallel digital output pin. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low, this pin is used to output DB14 of the conversion result. When $\overline{\text{PAR/SER SEL}} = 1$ and DB15/BYTE SEL = 1 the AD7606/AD7606-6/AD7606-4 will operate in parallel byte interface mode. In parallel byte mode HBEN pin used to select if the MSB byte or LSB byte of the conversion result is output first. When HBEN is = 1 the MSB byte is output first followed by the LSB byte. When HBEN is = 0 the LSB byte is output first followed by the MSB byte.
31 to 27	D.O.	DB[13: 9]	DB[13: 9]	DB[13: 9]	Parallel output data bits, Data Bit13 to Data Bit 9. When $\overline{\text{PAR/SER SEL}} = 0$, these pins act as three-state parallel digital input/output pins. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low, these pins are used to output DB13 to DB9 of the conversion result. When $\overline{\text{PAR/SER SEL}} = 1$, these pins should be tied to DGND.
24	D.O.	DB7/ D _{OUTA}	DB7/ D _{OUTA}	DB7/ D _{OUTA}	Parallel output Data Bit 7/ Serial interface data output pin D _{OUTA} . When $\overline{\text{PAR/SER SEL}} = 0$, this pins acts as a three-state parallel digital input/output pin. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low, this pin is used to output DB7 of the conversion result. When $\overline{\text{PAR/SER SEL}} = 1$, this pin functions as D _{OUTA} and outputs serial conversion data. See Conversion Control for further details. When operating in Parallel Byte mode DB7 will be the MSB of the byte.
25	D.O.	DB8/D _{OUT} B	DB8/D _{OUT} B	DB8/D _{OUT} B	Parallel output Data Bit 8/ Serial interface data output pin D _{OUTB} . When $\overline{\text{PAR/SER SEL}} = 0$, this pins acts as a three-state parallel digital input/output pin. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low, this pin is used to output DB8 of the conversion result. When $\overline{\text{PAR/SER SEL}} = 1$, this pin functions as D _{OUTB} and outputs serial conversion data. See Conversion Control for further details.
22 to 16	D.O.	DB[6: 0]	DB[6: 0]	DB[6: 0]	Parallel output data bits Data Bit 6 to Data Bit 0. When $\overline{\text{PAR/SER SEL}} = 0$, these pins act as three-state parallel digital input/output pins. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low, these pins are used to output DB6 to DB 0 of the conversion result. When $\overline{\text{PAR/SER SEL}} = 1$, these pins should be tied to DGND. When operating in parallel byte interface mode DB[7:0] will output the 16 bit conversion result in 2 RD operations. DB7 is the MSB and DB0 is the LSB.

TERMINOLOGY

Integral Nonlinearity

The maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a ½ LSB below the first code transition and full scale at ½ LSB above the last code transition.

Differential Nonlinearity

The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Bipolar Zero Code Error

The deviation of the midscale transition (all 1s to all 0s) from the ideal V_{IN} voltage, that is, AGND.

Bipolar Zero Code Error Match

The difference in bipolar zero code error between any two input channels.

Positive Full-Scale Error

The last transition (from 011 . . . 10 to 011 . . . 11 in twos complement coding) should occur for an analog voltage 1 1/2 LSB below the nominal full scale (9.999542 V for the ±10 V range and -4.999771 for the ±5V range). The positive full-scale error is the deviation of the actual level of the last transition from the ideal level.

Positive Full-Scale Error Match

The difference in positive full-scale error between any two input channels.

Negative Full-Scale Error

The first transition (from 100 . . . 00 to 100 . . . 01 in twos complement coding) should occur for an analog voltage 1/2 LSB above the negative full scale (-9.9998475 V for the ±10 V range and 4.999923 for the ±5V range). The negative full-scale error is the deviation of the actual level of the first transition from the ideal level.

Negative Full-Scale Error Match

The difference in negative full-scale error between any two input channels.

Track-and-Hold Acquisition Time

The track-and-hold amplifier returns to track mode at the end of the conversion. The track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±1 LSB, after the end of the conversion. See the Track-and-Hold for more details.

Signal-to-(Noise + Distortion) Ratio

The measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_s/2$, excluding dc). The ratio

depends on the number of quantization levels in the digitization process: the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$\text{Signal-to-(Noise + Distortion)} = (6.02 N + 1.76) \text{ dB}$$

Thus, for a 16-bit converter, this is 98 dB.

Total Harmonic Distortion (THD)

The ratio of the rms sum of the harmonics to the fundamental. For the AD7606, it is defined as

$$\text{THD(dB)} = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:

V_1 is the rms amplitude of the fundamental.

$V_2, V_3, V_4, V_5,$ and V_6 are the rms amplitudes of the second through sixth harmonics.

Peak Harmonic or Spurious Noise

The ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_s/2$, excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is determined by a noise peak.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, f_a and f_b , any active device with nonlinearities create distortion products at sum and difference frequencies of $m f_a \pm n f_b$, where $m, n = 0, 1, 2, 3$. Intermodulation distortion terms are those for which neither m nor n are equal to 0. For example, the second-order terms include $(f_a + f_b)$ and $(f_a - f_b)$, and the third-order terms include $(2f_a + f_b)$, $(2f_a - f_b)$, $(f_a + 2f_b)$, and $(f_a - 2f_b)$.

The AD7606 is tested using the CCIF standard in which two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves, and the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in decibels.

Power Supply Rejection (PSR)

Variations in power supply affect the full-scale transition but not the converter's linearity. Power supply rejection is the maximum change in full-scale transition point due to a change in power supply voltage from the nominal value. The power supply rejection ratio is defined as the ratio of the power in the ADC output at full-scale frequency, f , to the power of a 200 mV

p-p sine wave applied to the ADC's V_{DD} and V_{SS} supplies of frequency f_s

$$PSRR \text{ (dB)} = 10 \log (P_f/P_{f_s})$$

where:

P_f is equal to the power at frequency f in the ADC output.

P_{f_s} is equal to the power at frequency f_s coupled onto the V_{DD} and V_{SS} supplies.

Channel-to-Channel Isolation

Channel-to-channel isolation is a measure of the level of crosstalk between any two channels. It is measured by applying a full-scale, 10 kHz sine wave signal to all unselected input channels and determining the degree to which the signal attenuates in the selected channel with a 1 kHz signal.

TYPICAL PERFORMANCE CHARACTERISTICS

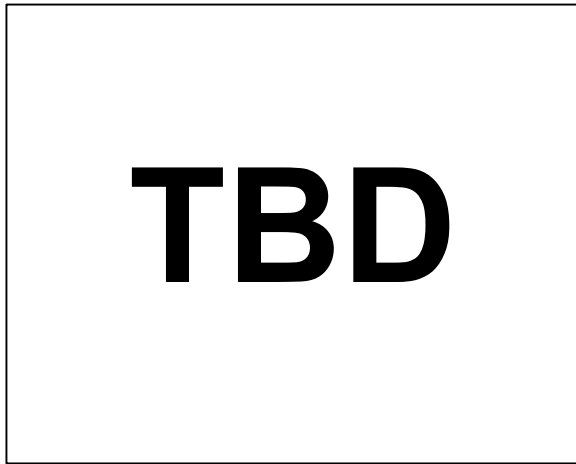


Figure 11 AD7606 FFT $\pm 10V$ range

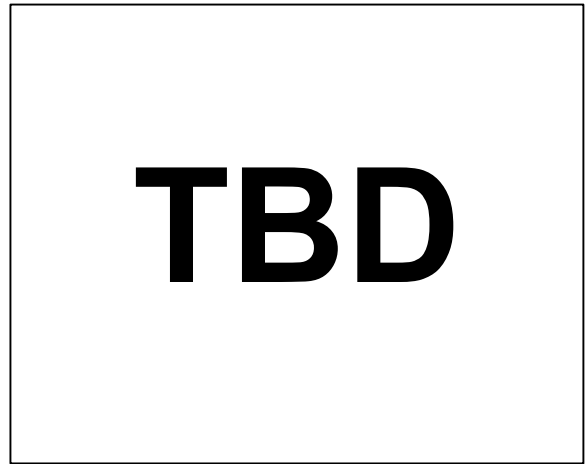


Figure 14 AD7606 typical DNL $\pm 10V$ range

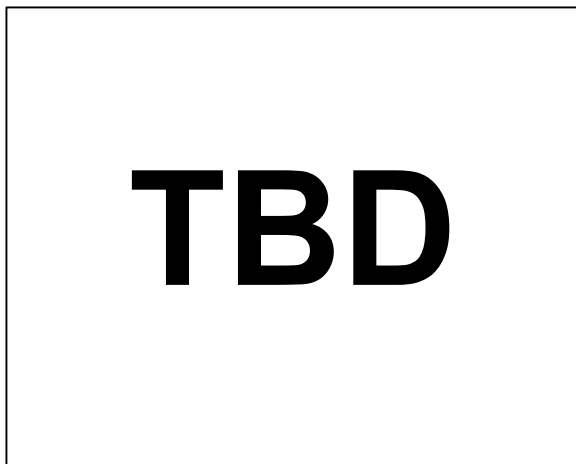


Figure 12 AD7606 FFT plot $\pm 5V$ range

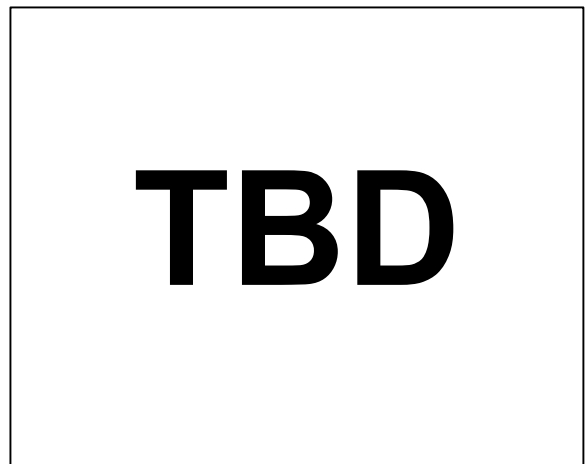


Figure 15 AD7606 typical INL $\pm 5V$ range

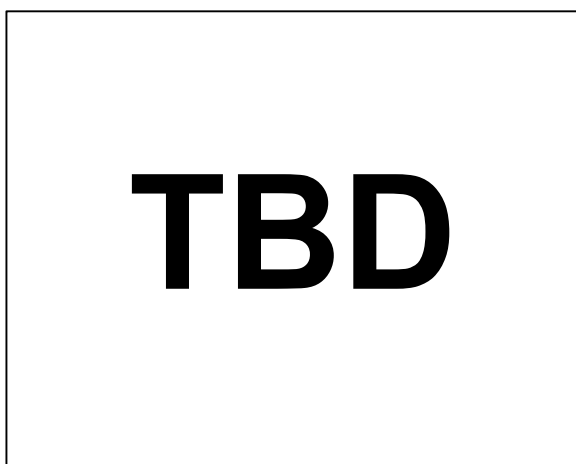


Figure 13 AD7606 typical INL $\pm 10V$ range

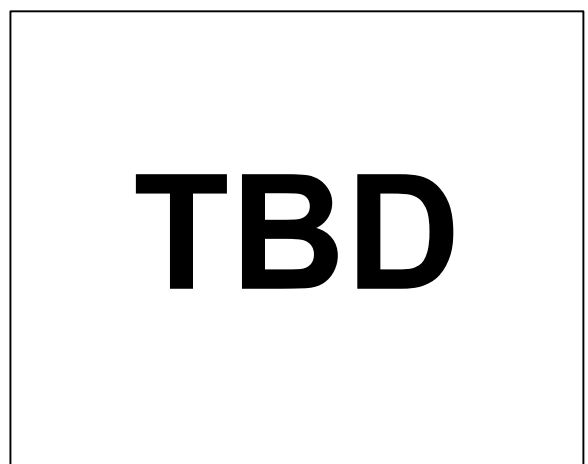


Figure 16 AD7606 typical DNL $\pm 5V$ range

TYPICAL PERFORMANCE CHARACTERISTICS

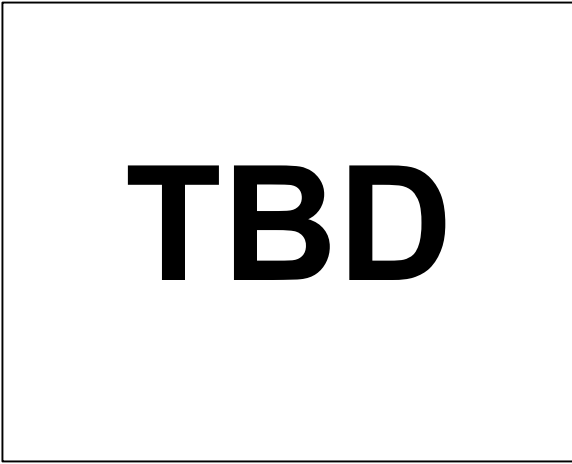


Figure 17 NFS and PFS error vs temperature

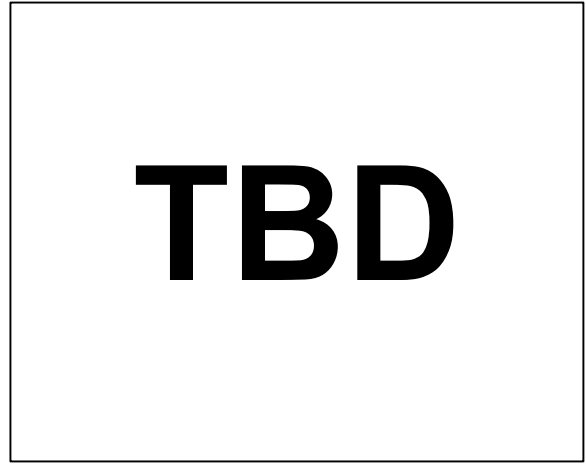


Figure 20 SNR vs Input Frequency

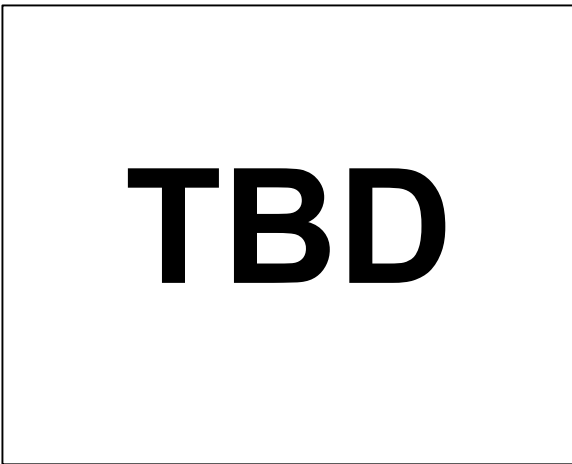


Figure 18 NFS and PFS error matching

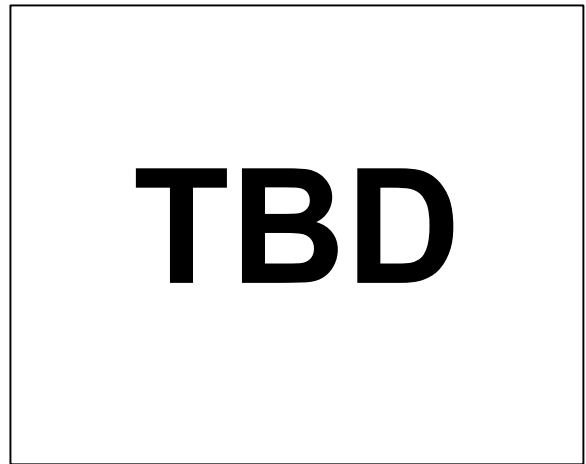


Figure 21 THD vs Input Frequency for various source impedances, $\pm 10V$ range

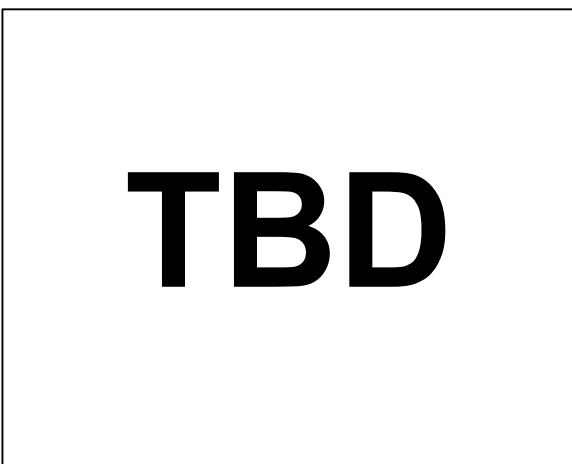


Figure 19 PFS and NFS error vs source resistance

TYPICAL PERFORMANCE CHARACTERISTICS

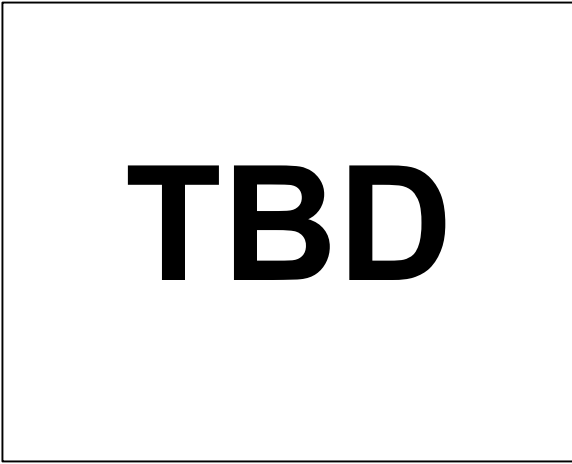


Figure 22 THD vs Input Frequency for various source impedances, $\pm 5v$ range

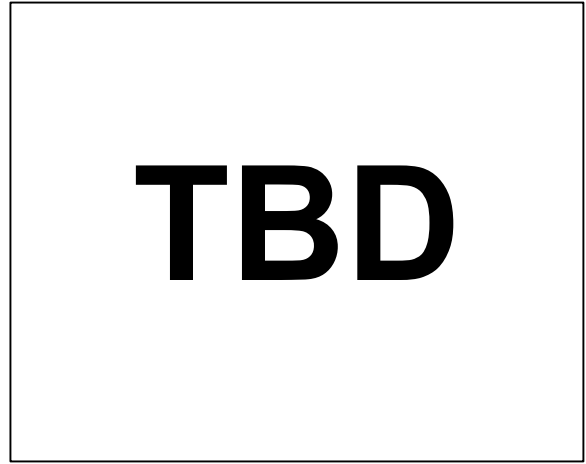


Figure 25 Channel to Channel isolation

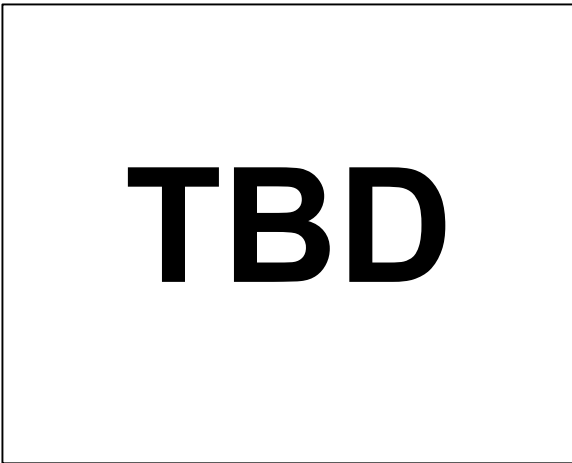


Figure 23 bipolar Zero Code error vs temperature

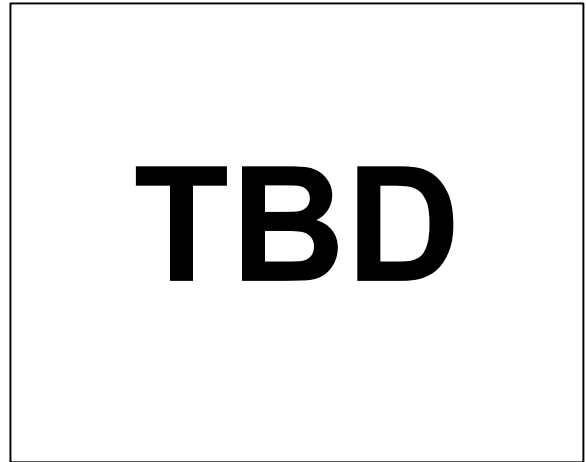


Figure 26 Histogram of codes

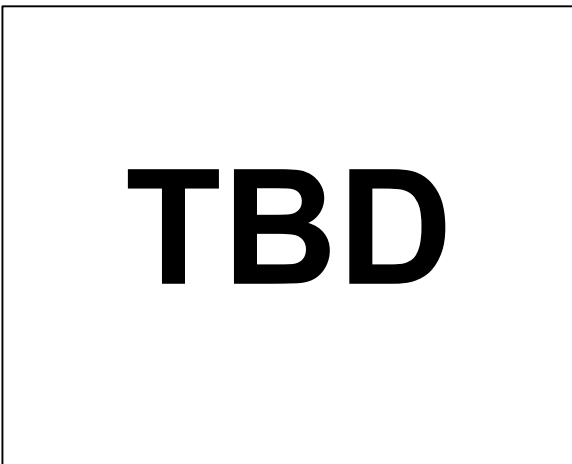


Figure 24 Bipolar Zero Code error matching between channels

TYPICAL PERFORMANCE CHARACTERISTICS

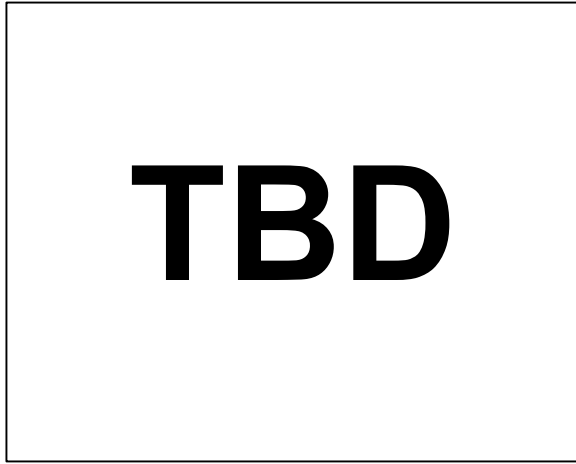


Figure 27 Reference output voltage vs Temperature for different supply Voltages

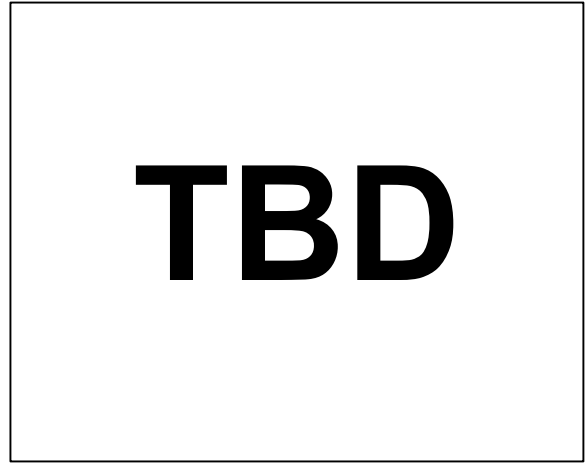


Figure 30 PSRR

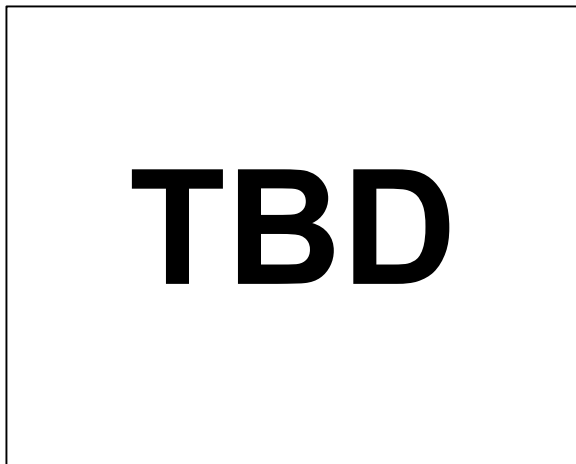


Figure 28 Analog Input current vs temperature for various supply voltages

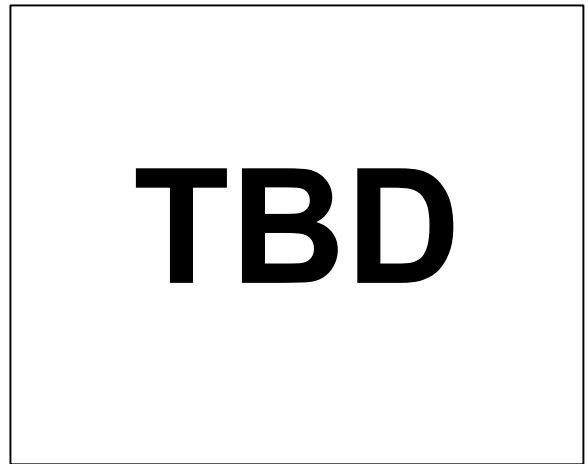


Figure 31 TBD

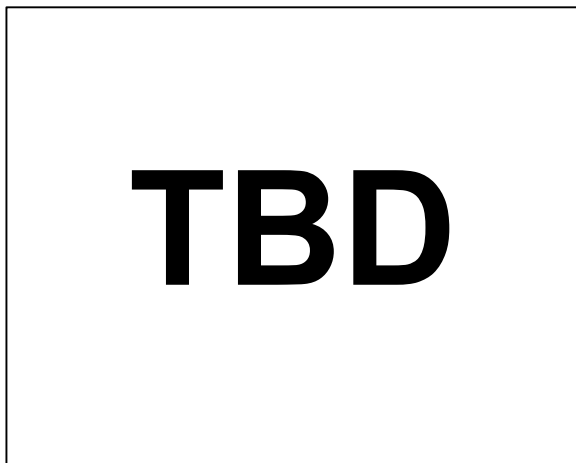


Figure 29 Supply Current vs Oversampling rate

THEORY OF OPERATION

CONVERTER DETAILS

The AD7606/AD7606-6/AD7606-4 is a data acquisition system that employs a high speed, low power, charge redistribution successive approximation analog-to-digital converter and allows the simultaneous sampling of eight/six/four analog input channels. The analog inputs on the AD7606/AD7606-6/AD7606-4 can accept true bipolar input signals. The RANGE pin is used to select either $\pm 10\text{V}$ or $\pm 5\text{V}$ as the input range. The AD7606/AD7606-6/AD7606-4 operates from a single 5V supply.

The AD7606/AD7606-6/AD7606-4 contains input clamp protection, input signal scaling amplifiers, 2nd order anti-aliasing filter, track-and-hold amplifiers, an on-chip reference, reference buffers, high speed analog-to-digital converter, digital filter and high speed parallel and serial interfaces. Sampling on the AD7606/AD7606-6/AD7606-4 is controlled using CONVST signals.

ANALOG INPUT

Analog Input Ranges

The AD7606/AD7606-6/AD7606-4 can handle true bipolar input voltages. The logic level on the RANGE pin determines the analog input range of all analog input channels. If this pin is tied to a logic high, the analog input range is $\pm 10\text{V}$ for all channels. If this pin is tied to a logic low, the analog input range is $\pm 5\text{V}$ for all channels. A logic change on this pin will have an immediate effect on the analog input range, however there will be a settling time in the order of 80 μs typically in addition to the normal acquisition time requirement. Recommended practice is to hardwire the range pin according to the desired input range for the system signals.

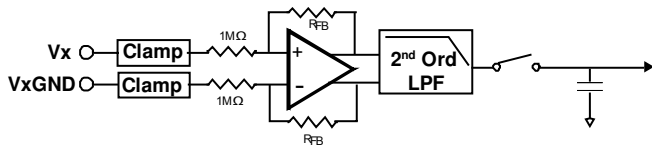


Figure 32 Analog Input Circuitry

Analog Input Impedance

The analog input impedance of the AD7606 is 1 M Ω . This is a fixed input impedance and does not vary with the AD7606 sampling frequency. This high analog input impedance eliminates the need for a driver amplifier in front of the AD7606 allowing for direct connection to the source or sensor. The elimination of the need for a driver amplifier removes the need for bipolar supplies from the signal chain, which are often a source of noise in a system.

Analog Input Clamp Protection

Figure 32 shows the analog input structure of the AD7606/AD7606-6/AD7606-4. Each AD7606 analog input contains clamp protection circuitry. Despite single 5V supply operation this analog input clamp protection allows for an input over voltage up to $\pm 16.5\text{V}$. Figure 33 shows the voltage vs current characteristic of the clamp circuit. For input voltages up to $\pm 16.5\text{V}$ no current flows in the clamp circuit. For input voltages above $\pm 16.5\text{V}$ the AD7606/AD7606-6/AD7606-4 clamp circuitry will turn on and clamp the analog input to $\pm 16.5\text{V}$. A series resistor should be placed on the analog input channels to limit the current to $\pm 10\text{mA}$ for input voltages above $\pm 16.5\text{V}$. In an application where there is a series resistance on an analog input channel VINx, a corresponding resistance is required on the analog input GND channel VxGND, see Figure 34. If there is no corresponding resistor on the VxGND channel this will result in a gain error on that channel.

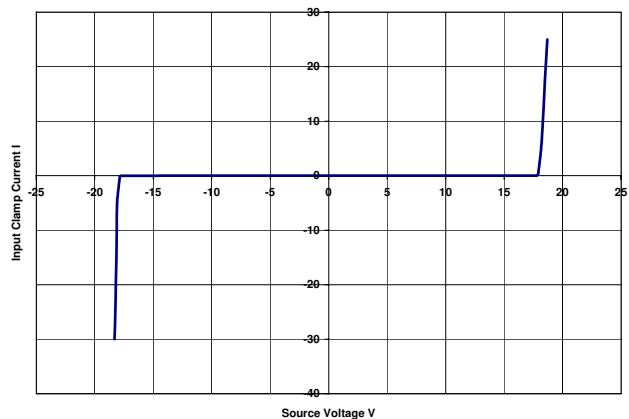


Figure 33 Input protection Clamp profile.

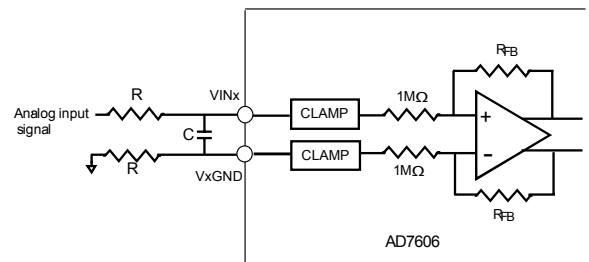


Figure 34. Input resistance matching on the analog input

Analog Input Anti-Aliasing Filter

An analog anti-alias filter is also provided on the AD7606/AD7606-6/AD7606-4. The filter is a 2nd order Butterworth. Figure 35 and Figure 36 show the frequency and phase response respectively of the analog anti-alias filter. In the ±5V range the -3dB frequency is typically 14 kHz. In the ±10V range the -3dB frequency is typically 22 kHz.



Figure 35 Analog Anti-Alias Filter Frequency Response

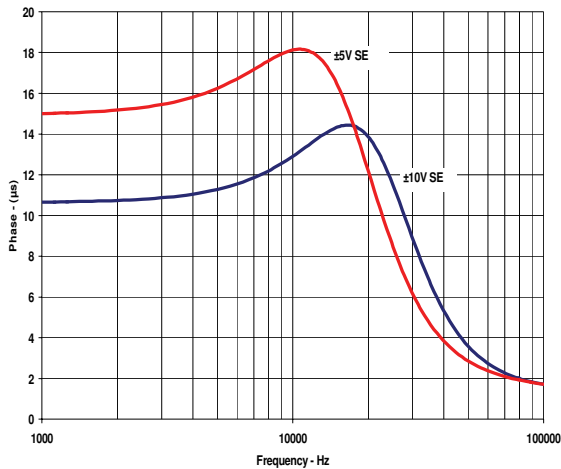


Figure 36. Analog Anti-Alias Filter Phase Response

Track-and-Hold Amplifiers

The track-and-hold amplifiers on the AD7606/AD7606-6/AD7606-4 allow the ADC to accurately acquire an input sine wave of full-scale amplitude to 16-bit resolution. The acquisition time for all input channels, t_{ACQ} , for the AD7606/AD7606-6/AD7606-4 is 1 µs. The track-and-hold amplifiers sample their respective inputs simultaneously on the rising edge of CONVST. The aperture time for the track-and-hold (that is, the delay time between the external CONVST signal and the track-and-hold actually going into hold) is TBD ns. This figure is well matched across all eight track-and-holds on one device and

from device to device. This allows more than one AD7606/AD7606-6/AD7606-4 device to be sampled simultaneously in a system. The end of the conversion process across all eight channels is indicated by the falling edge of BUSY, and it is at this point that the track-and-holds return to track mode and the acquisition time for the next set of conversions begins.

The conversion clock for the part is internally generated, and the conversion time for all channels is 4 µs on the AD7606, 3 µs on the AD7606-6 and 2 µs on the AD7606-4. The BUSY signal returns low after all eight conversions to indicate the end of the conversion process. On the falling edge of BUSY, the track-and-hold amplifiers return to track mode. New data can be read from the output register via the parallel, parallel byte or serial interface after BUSY goes low or alternatively data from the previous conversion may be read while BUSY is high. Reading data from the AD7606/AD7606-6/AD7606-4 while a conversion is in progress will have no effect on performance and will allow a faster throughput to be achieved.

ADC TRANSFER FUNCTION

The output coding of the AD7606/AD7606-6/AD7606-4 is twos complement. The designed code transitions occur midway between successive integer LSB values, that is, 1/2 LSB, 3/2 LSB. The LSB size is FSR/65,536 for the AD7606. The ideal transfer characteristic for the AD7606/AD7606-6/AD7606-4 is shown in Figure 37.

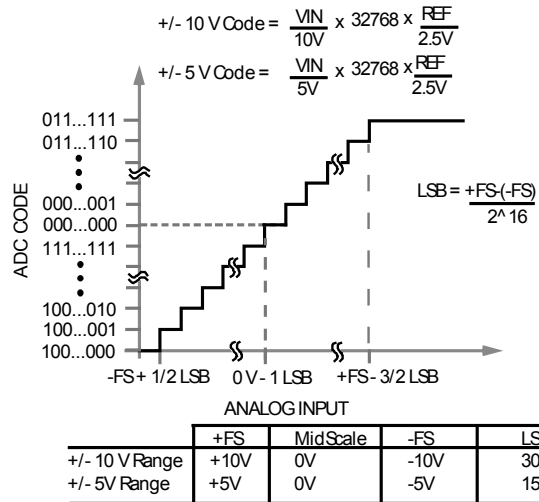


Figure 37. AD7606 Transfer Characteristic

The LSB size is dependent on the analog input range selected (see Table 6).

Table 6. LSB Size for Each Analog Input Range

	AD7606 Range	
Input Range	±10 V	±5 V
LSB Size	0.305 mV	0.152 mV
FS Range	20 V/65,536	10 V/65,536

INTERNAL/EXTERNAL REFERENCE

The AD7606/AD7606-6/AD7606-4 contains an on-chip 2.5 V bandgap reference. The REFIN/REFOUT pin allows access to the 2.5 V reference which generates the on-chip 4.55 V reference internally, or it allows an external reference of 2.5V to be applied to the AD7606/AD7606-6/AD7606-4. An externally applied reference of 2.5V will also be gained up to 4.55V using the internal buffer. This 4.55V buffered reference is the reference used by the SAR ADC.

The REF SELECT pin is a logic input pin which allows the user to select between the internal reference or and external reference. If this pin is set to logic high then the internal reference is selected and is enabled, if this pin is set to logic low then the internal reference is disabled and an external reference voltage must be applied to the REFIN/REFOUT pin. The internal reference buffer is always enabled. After a RESET, the AD7606/AD7606-6/AD7606-4 operates in the reference mode selected by the REF SELECT pin. Decoupling is required on the REFIN/REFOUT pin for both the internal or external reference options. A 10 μ F ceramic capacitor is required on the REFIN/REFOUT to ground close to the REFGND pins.

The AD7606/AD7606-6/AD7606-4 contains a reference buffer configured to gain the REF voltage up to \sim 4.55V as shown in Figure 38. The REFCAPA and REFCAPB pins must be shorted together externally and a ceramic capacitor of 10 μ F applied to REFGND to ensure the reference buffer is in closed loop operation. The reference voltage available at the REFIN/REFOUT pin is 2.5V.

When the AD7606/AD7606-6/AD7606-4 is configured in external reference mode the REFIN/REFOUT pin is a high input impedance pin. For applications using multiple AD7606 devices we recommend the following depending on the application requirements:

External reference mode: One ADR421 external reference can be used to drive the REFIN/REFOUT pins of all AD7606 devices, see Figure 40. In this configuration each AD7606/AD7606-6/AD7606-4 REFIN/REFOUT pin should be decoupled with a 100 nF decoupling capacitor.

Internal reference mode: One AD7606/AD7606-6/AD7606-4 device, configured to operate in the internal reference mode, could be used to drive the remaining AD7606/AD7606-6/AD7606-4 devices which are configured to operate in external reference mode, see Figure 39. The REFIN/REFOUT pin of the AD7606/AD7606-6/AD7606-4, configured in internal reference mode, should be decoupled using a 10 μ F ceramic decoupling capacitor. The other AD7606/AD7606-6/AD7606-4 devices, configured in external reference mode, should use a 100 nF decoupling capacitor on their REFIN/REFOUT pins.

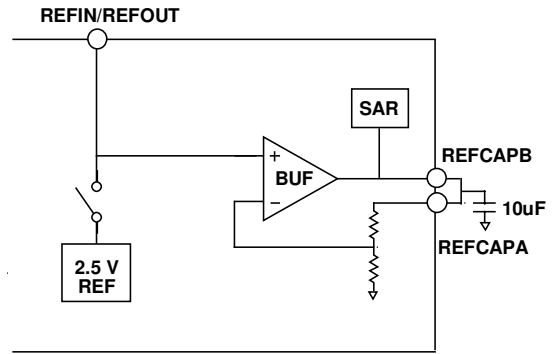


Figure 38 Reference Circuitry

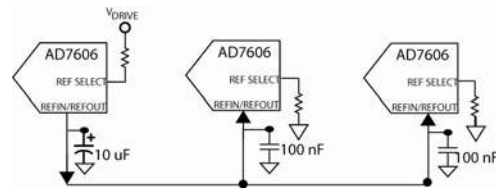


Figure 39. Internal Reference driving multiple AD7606 REFIN pins.

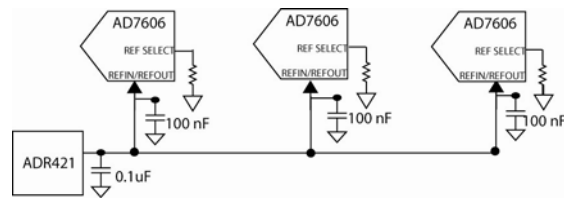


Figure 40. Single external Reference driving multiple AD7606 REFIN pins

AD7606/AD7606-6/AD7606-4

TYPICAL CONNECTION DIAGRAM

Figure 41 shows the typical connection diagram for the AD7606/AD7606-6/AD7606-4. There are four AV_{CC} supply pins on the part which can be tied together and decoupled using a 100nF cap at each supply pin and a 10 μ F capacitor at the supply source. The AD7606/AD7606-6/AD7606-4 can operate with the internal reference or an externally applied reference. In this configuration, the AD7606 is configured to operate with the internal reference. When using a single AD7606/AD7606-6/AD7606-4 device on the board the REFIN/REFOUT pin should be decoupled with a 10 μ F capacitor, in an application with multiple AD7606 /AD7606-6/AD7606-4 devices see Internal/external Reference section. The REFCAPA and REFCAPB pins are shorted together and decoupled with a 10 μ F ceramic capacitor.

The V_{DRIVE} supply is connected to the same supply as the processor. The voltage on V_{DRIVE} controls the voltage value of the output logic signals. For layout, decoupling and grounding hints see AD7606/AD7606-6/AD7606-4 layout guidelines.

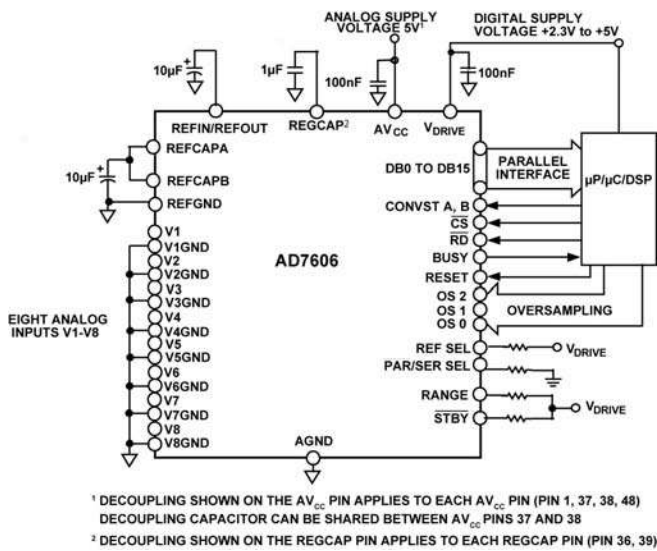


Figure 41 AD7606 Typical Connection Diagram

POWER-DOWN MODES

There are two power-down modes available on the AD7606/AD7606-6/AD7606-4. The STBY pin controls whether the AD7606/AD7606-6/AD7606-4 is in normal mode or one of the two power-down modes. The two power-down modes available are Standby mode and Shutdown mode. The power-down mode is selected through the state of the RANGE pin when the STBY pin is low. Table 7 shows the configurations required to choose the desired power-down mode. When the AD7606/AD7606-6/AD7606-4 is placed in Standby mode the

current consumption is 2mA max and power up time is in the order of 100 μ s as the capacitor on the RefcapA/ RefCapB pins must charge up. In Standby mode the on chip reference and regulators remain powered up and the amplifiers and ADC core are powered down. When the AD7606/AD7606-6/AD7606-4 is placed in Shutdown mode the current consumption is 1 μ A max and power up time is also in the order of 11ms. In Shutdown mode all circuitry is powered down. When the AD7606/AD7606-6/AD7606-4 is powered up from Shutdown mode, a RESET signal must be applied to the AD7606/AD7606-6/AD7606-4 after the required power up time has elapsed.

Table 7 Power-down Mode Selection

Power-down mode	STBY	RANGE
Standby	0	1
Shutdown	0	0

CONVERSION CONTROL

Simultaneous sampling on all analog input channels

The AD7606 /AD7606-6/AD7606-4 allows simultaneous sampling of all analog input channels. All channels are sampled simultaneously when both CONVST pins (CONVST A, CONVST B) are tied together. A single CONVST signal is used to control both inputs. The rising edge of this common CONVST signal initiates simultaneous sampling on all analog input channels (V1 to V8 for the AD7606, V1 to V6 for the AD7606-6 and V1 to V4 for the AD7606-4).

The AD7606 contains an on-chip oscillator that is used to perform the conversions. The conversion time for all ADC channels, t_{CONV} . The BUSY signal indicates to the user when conversions are in progress, so when the rising edge of CONVST is applied, BUSY goes logic high, and transitions low at the end of the entire conversion process. The falling edge of the BUSY signal is used to place all eight track-and-hold amplifiers back into track mode. The falling edge of BUSY also indicates that the new data may now be read from the parallel bus DB[15:0], serial data lines DOUTA and DOUTB or using the parallel byte bus DB[7:0].

Simultaneously sampling two sets of channels

The AD7606/AD7606-6/AD7606-4 also allows the analog input channels to be sampled simultaneously in two sets. This can be used in Power Line protection and measurement systems to compensate for phase differences between PT and CT transforms.

This is accomplished by pulsing the two CONVST pins independently and is only possible if oversampling is not in use. CONVST A is used to initiate simultaneous sampling the first set of channels (V1 to V4 for the AD7606, V1 to V3 for the AD7606-6 and V1 to V2 for the AD7606-4), CONVST B is used

to initiate simultaneous sampling on the second set of analog input channels, (V5 to V8 for the AD7606, V4 to V6 for the AD7606-6 and V3 to V4 for the AD7606-4) as illustrated in Figure 42. On the rising edge of CONVST A, the track-and-hold amplifiers for the first set of channels are placed into hold mode. On the rising edge of CONVST B, the track-and-hold amplifiers for the second set of channels are placed into hold mode. The conversion process begins once both rising edges of CONVST have occurred, so BUSY will go high on the rising edge of the later CONVST signal. The falling edge of BUSY also

indicates that the new data may now be read from the parallel bus DB[15:0], serial data lines DOUTA and DOUTB or using the parallel byte bus DB[7:0].

There is no change to the data read process when using two separate CONVST signals.

Connect all unused analog input channel to AGND. The results for any unused channels will still be included in the data read as all channels are always converted.

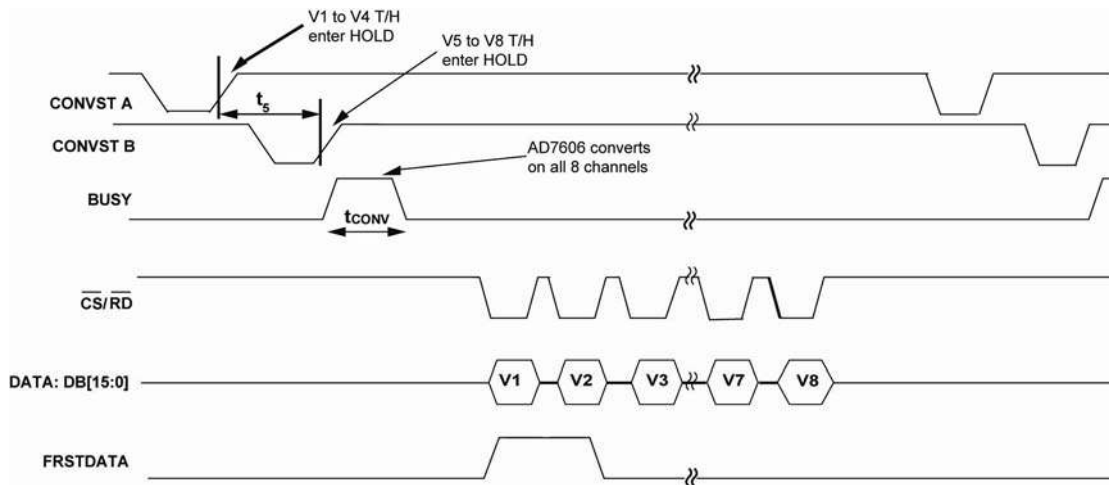


Figure 42. Simultaneous Sampling on channel sets using independent CONVST A/B signals – parallel mode

DIGITAL INTERFACE

The AD7606/AD7606-6/AD7606-4 provides three interface options, a parallel interface, parallel byte interface and a high-speed serial interface. The required interface mode is selected via the $\overline{\text{PAR/SER SEL}}$ and DB15 pins.

Table 8. Interface Mode selection

$\overline{\text{PAR/SER SEL}}$	DB15	Interface Mode
0	0	Parallel interface mode
1	0	Serial interface mode
1	1	Parallel byte mode

The operation of the interface modes is discussed in the following sections.

PARALLEL INTERFACE ($\overline{\text{PAR/SER/BYTE SEL}} = 0$)

Data can be read from the AD7606/AD7606-6/AD7606-4 via the parallel data bus with standard $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals. To read the data over the parallel bus, the $\overline{\text{PAR/SER/BYTE SEL}}$ pin should be tied low. The $\overline{\text{CS}}$ and $\overline{\text{RD}}$ input signals are internally gated to enable the conversion result onto the data bus. The data lines DB0 to DB15 leave their high impedance state when both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are logic low.

The rising edge of the $\overline{\text{CS}}$ input signal tri-states the bus and the falling edge of the $\overline{\text{CS}}$ input signal takes the bus out of the high impedance state. $\overline{\text{CS}}$ is the control signal that enables the data lines, it is the function that allows multiple AD7606/AD7606-6/AD7606-4 devices to share the same parallel data bus.

The $\overline{\text{CS}}$ signal can be permanently tied low, and the $\overline{\text{RD}}$ signal can be used to access the conversion results as shown in Figure 4. A read operation of new data can take place after the $\overline{\text{BUSY}}$ signal goes low (Figure 2), or alternatively a read operation of data from the previous conversion process can take place while $\overline{\text{BUSY}}$ is high (Figure 3).

The $\overline{\text{RD}}$ pin is used to read data from the output conversion results register. Applying a sequence of $\overline{\text{RD}}$ pulses to the AD7606/AD7606-6/AD7606-4 $\overline{\text{RD}}$ pin clocks the conversion results out from each channel onto the parallel output bus

DB[15:0] in ascending order. The first $\overline{\text{RD}}$ falling edge after $\overline{\text{BUSY}}$ goes low clocks out the conversion result from channel V1, the next $\overline{\text{RD}}$ falling edge updates the bus with the V2 conversion result and so on. On the AD7606, the 8th falling edge of $\overline{\text{RD}}$ clocks out the conversion result for channel V8. When the $\overline{\text{RD}}$ signal is logic low, it enables the data conversion result from each channel to be transferred to the digital host (DSP, FPGA).

When there is only one AD7606/AD7606-6/AD7606-4 in a system/board and it does not share the parallel bus, data can be read using just one control signal from the digital host. The $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals can be tied together as shown in Figure 5. In this case the data bus comes out of tri-state on the falling edge of $\overline{\text{CS/RD}}$. The combined $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signal allows the data to be clocked out of the AD7606/AD7606-6/AD7606-4 and to be read by the digital host. In this case $\overline{\text{CS}}$ is used to frame the data transfer of each data channel.

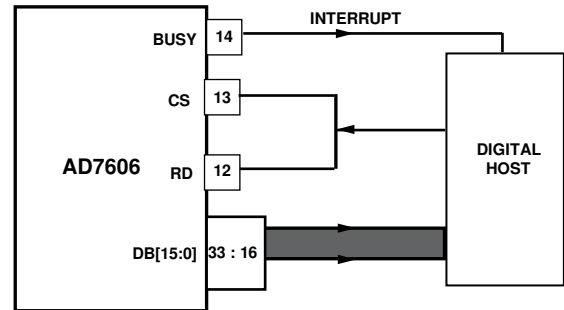


Figure 43 AD7606 interface diagram: One AD7606 using the parallel bus; $\overline{\text{CS}}$ and $\overline{\text{RD}}$ shorted together.

AD7606/AD7606-6/AD7606-4

Parallel Byte Mode ($\overline{\text{PAR/SER/BYTE SEL}} = 1, \text{DB15} = 1$)

Parallel byte interface mode operates similarly to the parallel interface mode except that each channel conversion result is read out in 2 eight bit transfers, therefore 16 $\overline{\text{RD}}$ pulses are required to read all 8 conversion results from the AD7606. For the AD7606-6 12 $\overline{\text{RD}}$ pulses are required and on the AD7606-4 8 $\overline{\text{RD}}$ pulses are required to read all the channel results. To configure the AD7606/AD7606-6/AD7606-4 to operate in parallel byte mode the $\overline{\text{PAR/SER/BYTE SEL}}$ and DB15 should be tied to logic high, see Table 8. In parallel byte mode DB[7:0] are used to transfer the data to the digital host. DB0 is the LSB of the data transfer and DB7 is the MSB of the data transfer. In parallel byte mode DB 14 acts as a HBEN pin. When DB14 is tied to logic high the MSB byte of the conversion result will be output first followed by the LSB byte of the conversion result. When DB14 is tied to logic low the LSB byte of the conversion result will be output first followed by the MSB byte of the conversion result. The FRSTDATA pin will remain high until the entire 16 bits of the conversion result from V1 is read from the AD7606/AD7606-6/AD7606-4.

Serial Interface ($\overline{\text{PAR/SER SEL}} = 1$)

To read data back from the AD7606 over the serial interface, the $\overline{\text{PAR/SER/BYTE SEL}}$ pin should be tied high. The $\overline{\text{CS}}$ and SCLK signals are used to transfer data from the AD7606. The AD7606 has two serial data output pins, D_{OUTA}, and D_{OUTB}. Data can be read back from the AD7606/AD7606-6/AD7606-4 using one or both of these DOUT lines. For the AD7606 conversion results from channels V1 to V4 first appear on D_{OUTA} while conversion results from channels V5 to V8 first appear on D_{OUTB}, for the AD7606-6 conversion results from channels V1 to V3 first appear on D_{OUTA} while conversion results from channels V4 to V6 first appear on D_{OUTB} and for the AD7606-4 conversion results from channels V1 and V2 first appear on D_{OUTA} while conversion results from channels V3 and V4 first appear on D_{OUTB}.

The $\overline{\text{CS}}$ falling edge takes the data output lines D_{OUTA} and D_{OUTB} out of tri-state and clocks out the MSB of the conversion result. The rising edge of SCLK clocks all subsequent data bits onto the serial data outputs D_{OUTA} and D_{OUTB}. The $\overline{\text{CS}}$ input can be held low for the entire serial read or it can be pulsed to frame each channel read of 16 SCLK cycles.

Figure 44 shows a read of eight simultaneous conversion results using two DOUT lines on the AD7606. In this case, a 64 SCLK transfer is used to access data from the AD7606/AD7606-6/AD7606-4 and $\overline{\text{CS}}$ is held low to frame the entire 64 SCLK cycles. Data can also be clocked out using just one DOUT line,

in which case D_{OUTA} is recommended to access all conversion data as the channel data will be output in ascending order. For the AD7606 to access all eight conversion results on one DOUT line a total of 128 SCLK cycles are required. These 128 SCLK cycles can be framed by one $\overline{\text{CS}}$ signal or each group of 16 SCLK cycles can be individually framed by the $\overline{\text{CS}}$ signal. The disadvantage of using just one DOUT line is that the throughput rate is reduced if reading after conversion. The unused DOUT line should be left unconnected in serial mode. For the AD7606 if D_{OUTB} is to be used as a single DOUT line then the channel results will be output in the order V5, V6, V7, V8, V1, V2, V3, V4, however the FRSTDATA indicator will return low once V5 is read on D_{OUTB}. For the AD7606-6 and the AD7606-4 if D_{OUTB} is to be used as a single DOUT line then the channel results will be output in the order V4, V5, V6, V1, V2, V3 for the AD7606-6 and V3, V4, V1, V2 for the AD7606-4.

Figure 6 shows the timing diagram for reading one channel of data, framed by the $\overline{\text{CS}}$ signal, from the AD7606/AD7606-6/AD7606-4 in serial mode. The SCLK input signal provides the clock source for the serial read operation. The $\overline{\text{CS}}$ goes low to access the data from the AD7606/AD7606-6/AD7606-4. The falling edge of $\overline{\text{CS}}$ takes the bus out of three-state and clocks out the MSB of the 16-bit conversion result. This MSB is valid on the first falling edge of the SCLK after the $\overline{\text{CS}}$ falling edge. The subsequent 15 data bits are clocked out of the AD7606/AD7606-6/AD7606-4 on the SCLK rising edge. Data is valid on the SCLK falling edge. Sixteen clock cycles must be provided to the AD7606/AD7606-6/AD7606-4 to access each conversion result.

The FRSTDATA output signal indicates when the first channel, V1, is being read back. When the $\overline{\text{CS}}$ input is high the FRSTDATA output pin is in three-state. In serial mode, the falling edge of $\overline{\text{CS}}$ takes FRSTDATA out of three-state and sets the FRSTDATA pin high indicating that the result from V1 is available on the D_{OUTA} output data line. The FRSTDATA output returns to a logic low following the sixteenth SCLK falling edge. If all channels are read on D_{OUTB} then the FRSTDATA output will not go high when V1 is being output on this serial data output pin. It only goes high when V1 is available on D_{OUTA} (and this is when V5 is available on D_{OUTB} for the AD7606).

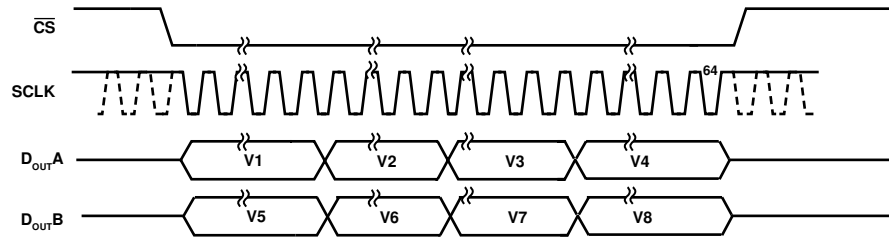


Figure 44. AD7606 Serial Interface with two DOUT Lines

READING DURING CONVERSION

Data may be read from the AD7606/AD7606-6/AD7606-4 while BUSY is high and conversions are in progress. This will not affect the performance of the converter and allows a faster throughput rate to be achieved. A parallel, parallel byte or serial read may be performed during conversions and when oversampling may be in use or not. Figure 3 shows the timing diagram for reading while BUSY is high in parallel or serial

mode. Reading during conversions allows the full throughput rate to be achieved when using the serial interface.

Data can be read from the AD7606 at any time other than on the falling edge of BUSY, as this is when the output data registers get updated with the new conversion data, t_6 outlined in Table 2 should be observed in this condition.

DIGITAL FILTER

The AD7606/AD7606-6/AD7606-4 contains an optional digital filter. This digital filter is a 1st order sinc filter. This digital filter should be used in applications where slower throughput rates are used or where higher signal to noise ratio or dynamic range is desirable. The over sampling ratio of the digital filter is controlled using the oversampling pins OS[2:0], see Table 9. OS 2 is the MSB control bit while OS 0 is the LSB control bit. Table 9 provides the over-sampling bit decoding to select the different over-sample rates. The OS pins are latched on the falling edge of BUSY. This will set the over sampling rate for the next

conversion, see Figure 45. In addition to the over-sampling function, the output result is decimated to 16-bit resolution.

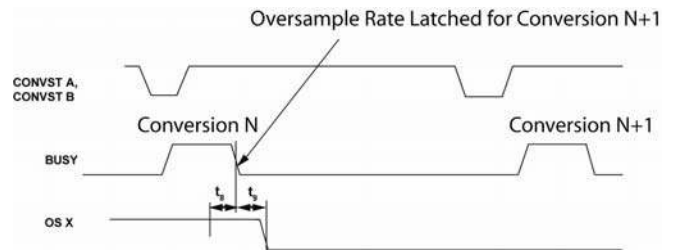


Figure 45. OS pin timing

Table 9 Over-sample Bit Decoding

OS [2:0]	OS Ratio	SNR 5V range dB	SNR 10V range dB	3 dB BW 5V range Hz	3 dB BW 10V range Hz	Max Throughput CONVST frequency
000	No OS	89.58	90	14.5k	22k	200k
001	2	TBD	TBD	14k	20k	100k
010	4	TBD	TBD	12.5k	16.5k	50k
011	8	TBD	TBD	9k	10.4k	25k
100	16	TBD	TBD	5.3k	5.5k	12.5k
101	32	TBD	TBD	2.75k	2.75k	6.25k
110	64	TBD	TBD	1.38k	1.38k	3.125k
111	Invalid					

If the OS pins are set to select an OS ratio of 8, the next CONVST rising edge will take the first sample for each channel and the remaining 7 samples for all channels are taken with an internally generated sampling signal. These samples are then averaged to yield an improvement in SNR performance. Table 9 shows typical SNR performance for both the ± 10 V and the ± 5 V range. As the table indicates, there is an improvement in SNR as the OS ratio increases. As the OS ratio is increased the 3 dB frequency is reduced and the allowed sampling frequency is also reduced. In an application where the required sampling frequency is 10 kSPS an OS ratio of up to 16 can be used. In this case the application will see an improvement in SNR but the input 3 dB bandwidth will be limited to ~ 5 kHz.

The CONVST A and CONVST B pins must be tied/ driven together when over-sampling is turned on. When the over-sampling function is turned on, then the BUSY high time for the conversion process will be seen to extend. The actual BUSY high time will depend on the over-sampling rate selected; the

higher the over-sampling rate, the longer the BUSY high, or total conversion time, see Table 2.

Figure 46 shows that the conversion time can be seen to extend as the over-sampling rate is increased. Figure 46 shows the BUSY signal lengthening for the different over-sampling rates. For example, a sampling frequency of 10 kSPS yields a cycle time of 100 μ s. Figure 46 shows OS x 4 and OS x 8, for 10 kSPS example there is adequate cycle time to continue to increase the over-sampling rate further. In an application where the initial sampling or throughput rate is at 200kSPS for example, then if over-sampling is turned on, then the throughput rate will have to be reduced to accommodate the longer conversion time and to allow for the read. The read may be performed during the BUSY high time in order to achieve the fastest throughput rate possible when over-sampling is turned on. The falling edge of BUSY is used to update the output data registers with the new conversion data and hence the reading of conversion data should occur on this edge. Figure 47 to Figure 50 illustrates the effect of over-sampling on

the code spread in a DC histogram plot. As the over-sample rate is increased, the spread of codes is reduced.

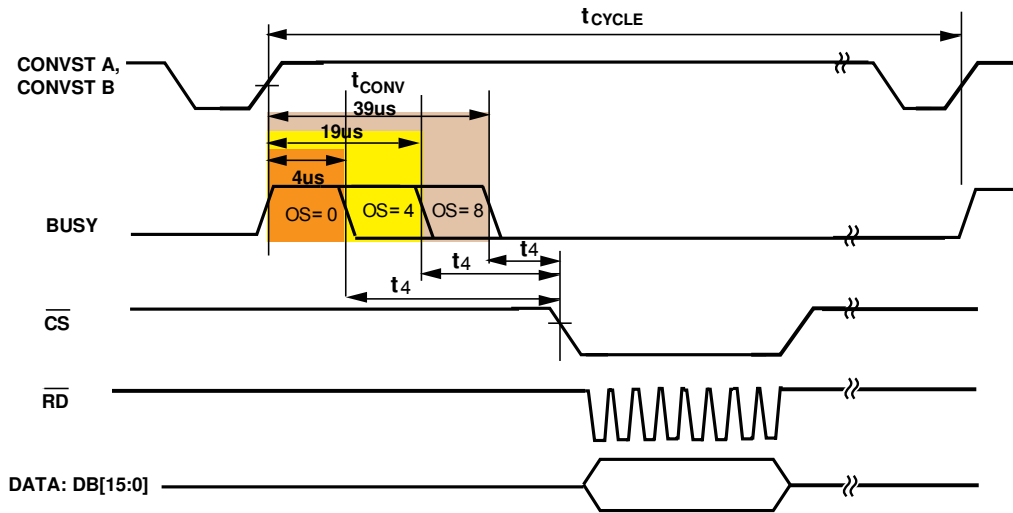


Figure 46 AD7606 - No Oversampling, OverSampling x 4 and OverSampling x 8 using read after conversion

On the AD7606/AD7606-6/AD7606-4 when the oversampling mode is selected this has the effect of adding a digital filter function after the ADC. The different oversampling rates and the CONVST sampling frequency will produce different digital filter frequency profiles.

Figure 51, Figure 52 and Figure 53 shows the digital filter frequency profiles for sampling rates of 4, 16 and 64 respectively. The combination of the analog anti-alias filter and the oversampling digital filter can be used to eliminate and reduce the complexity of the design of the filter before the AD7606/AD7606-6/AD7606-4. The digital filtering combines steep roll-off and linear phase response.

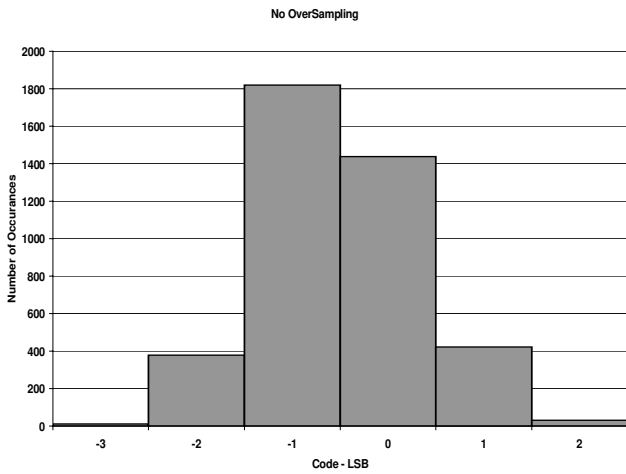


Figure 47. Histogram of codes – No OS – (6 codes)

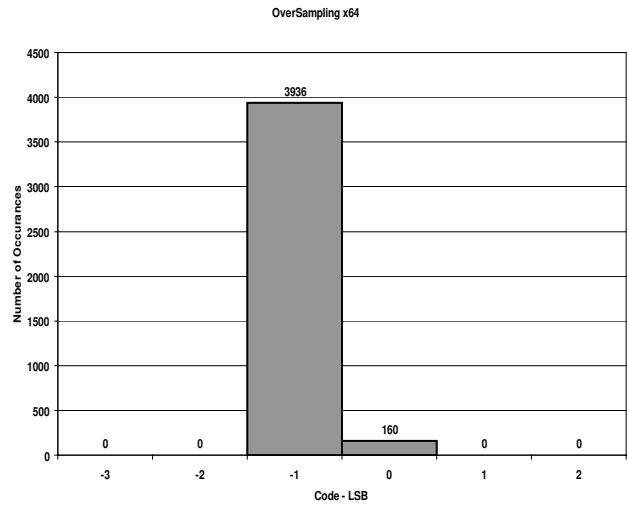


Figure 50. Histogram of codes – OS x 64 (2 codes)

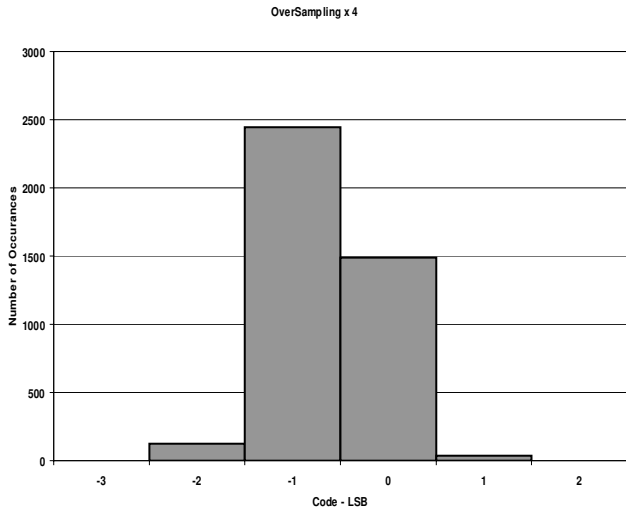


Figure 48 Histogram Of Codes – OS x 4.(4 codes)

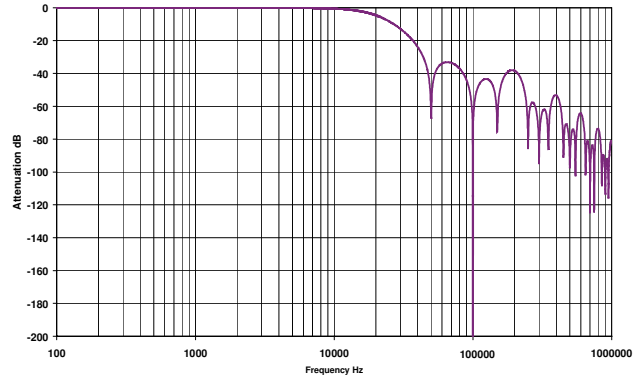


Figure 51. Digital Filter response for OS4

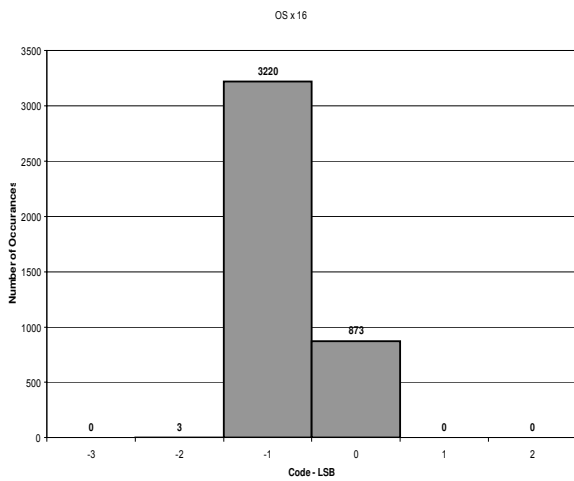


Figure 49. Histogram of codes – OS x 16 (3 codes)

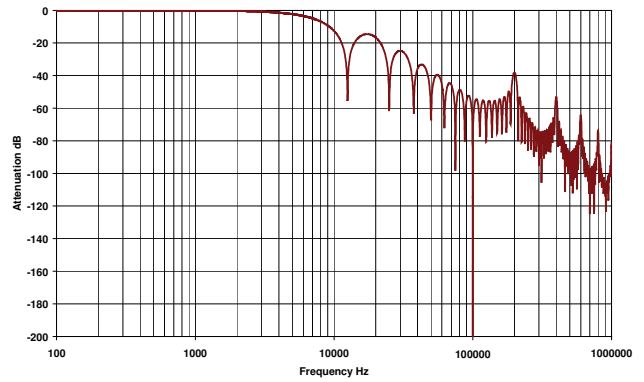


Figure 52. Digital filter response for OS 16

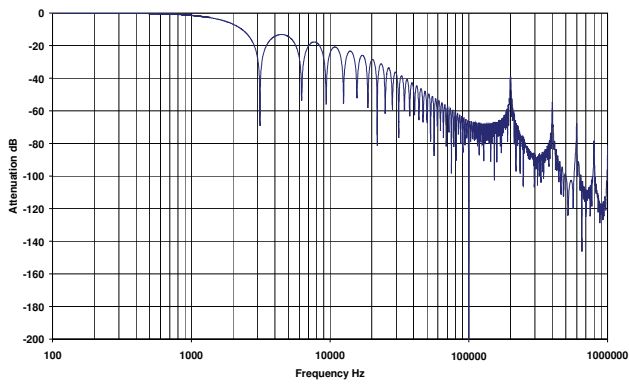


Figure 53. Digital filter response for OS 64

AD7606/AD7606-6/AD7606-4

AD7606/AD7606-6/AD7606-4 LAYOUT GUIDELINES

The printed circuit board that houses the AD7606/AD7606-6/AD7606-4 should be designed so that the analog and digital sections are separated and confined to different areas of the board.

At least one ground plane should be used. It can be common or split between the digital and analog sections. In the case of the split plane, the digital and analog ground planes should be joined in only one place, preferably as close as possible to the AD7606/AD7606-6/AD7606-4.

If the AD7606/AD7606-6/AD7606-4 is in a system where multiple devices require analog-to-digital ground connections, the connection should still be made at only one point, a star ground point, which should be established as close as possible to the AD7606/AD7606-6/AD7606-4. Good connections should be made to the ground plane. Avoid sharing one connection for multiple ground pins. Individual vias or multiple vias to the ground plane should be used for each ground pin.

Avoid running digital lines under the devices because doing so couples noise onto the die. The analog ground plane should be allowed to run under the AD7606 to avoid noise coupling. Fast-switching signals like CONVSTA, CONVSTB or clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and they should never run near analog signal paths. Crossover of digital and analog signals should be avoided. Traces on layers in close proximity on the board should run at right angles to each other to reduce the effect of feedthrough through the board.

The power supply lines to the AV_{CC} and V_{DRIVE} pins on the AD7606/AD7606-6/AD7606-4 should use as large a trace as possible to provide low impedance paths and reduce the effect of glitches on the power supply lines. Where possible supply planes should be used. Good connections should be made between the AD7606 supply pins and the power tracks on the board; this should involve the use of a single via or multiple vias for each supply pin.

Good decoupling is also important to lower the supply impedance presented to the AD7606/AD7606-6/AD7606-4 and to reduce the magnitude of the supply spikes. The decoupling capacitors should be placed close to, ideally right up against, these pins and their corresponding ground pins. The decoupling capacitors for the REFIN/REFOUT pin and the REFCAPA and REFCAPB pins should be placed as close as possible to their respective AD7606/AD7606-6/AD7606-4 pins and where possible they should be placed on the same side of the board as the AD7606 device. Figure 54 shows the recommended decoupling on the top layer of the AD7606 board. Figure 55 shows bottom layer decoupling. Bottom layer decoupling is for the 4 AV_{CC} pins and the V_{DRIVE} pin.

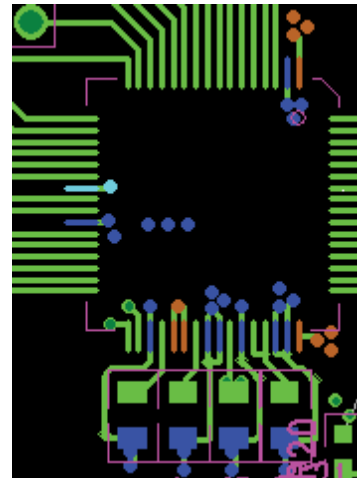


Figure 54. Top layer decoupling REFIN/REFOUT, REFCAP,A, REFCAPB and REGCAP pins

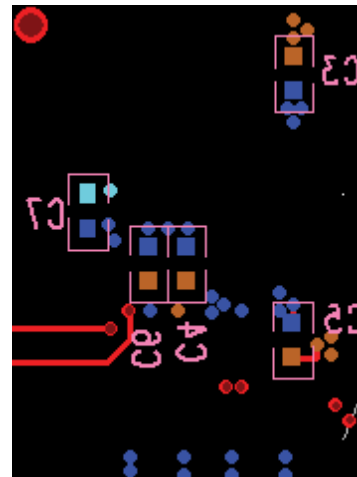


Figure 55. Bottom Layer decoupling

In a system that contains multiple AD7606/AD7606-6/AD7606-4 devices, to ensure good device-to-device performance matching, a symmetrical layout between the AD7606/AD7606-6/AD7606-4 devices is important. Figure 56 shows a layout with 2 AD7606/AD7606-6/AD7606-4 devices. The AV_{CC} supply plane runs to the right of both devices. The V_{DRIVE} supply track runs to the left of the 2 AD7606/AD7606-6/AD7606-4 devices. The reference chip is positioned between both AD7606/AD7606-6/AD7606-4 devices and the reference voltage track runs north to pin 42 of U1 and south to pin 42 of U2. A solid ground plane is used. These symmetrical layout principles can be applied to a system that contains more than 2 AD7606 devices. The AD7606/AD7606-6/AD7606-4 devices can be placed in a North South direction with the reference voltage located midway between the AD7606/AD7606-6/AD7606-4 devices with the reference track running in the north south direction similar to Figure 56.

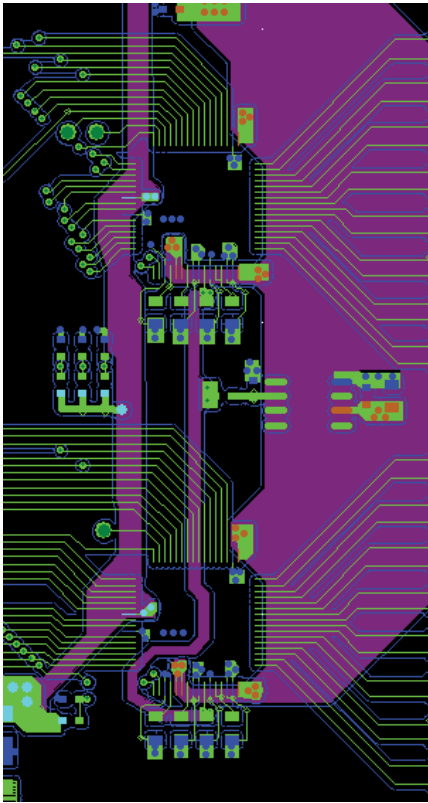


Figure 56. Multiple AD7606 layout, Top layer and Supply plane layer.

OUTLINE DIMENSIONS

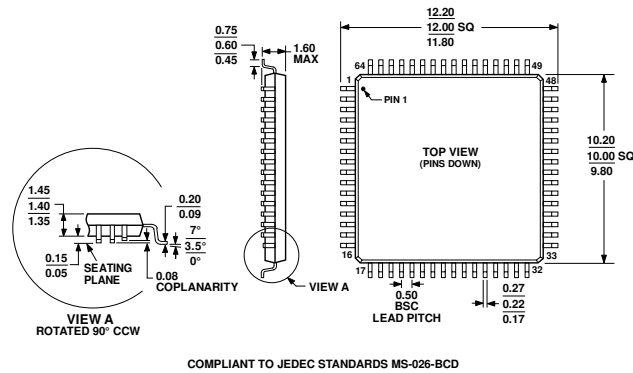


Figure 57 64-Lead Low Profile Quad Flat Package [LQFP]

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7606BSTZ ¹	-40°C to +85°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
AD7606BSTZ-RL ¹	-40°C to +85°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
AD7606BSTZ-6 ¹	-40°C to +85°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
AD7606BSTZ-6RL ¹	-40°C to +85°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
AD7606BSTZ-4 ¹	-40°C to +85°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
AD7606BSTZ-4RL ¹	-40°C to +85°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
EVAL-AD7606EDZ	-40°C to +85°C	Evaluation Board for the AD7606	
CED1Z		Converter Evaluation Development	

¹ Z = RoHS Compliant Part.

NOTES